Stable Phosphorus Passivated SiO_2/4H-SiC Interface Using Thin Oxides

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Keywords: Silicon carbide, interface-passivation, bias-temperature stress, stability

Abstract: The NO (nitric oxide) passivation process for 4H-SiC MOSFETs (silicon carbide metal-oxide-semiconductor filed effect transistors) effectively reduces the interface trap density and increases the inversion channel mobility from less that 10 to around 35cm^2/V.s, only 5% of the bulk mobility. Recent results on the phosphorous passivation of the SiO_2/4H-SiC interface have shown that it improves the mobility to about 90 cm^2/V.s. Phosphorous passivation converts oxide (SiO_2) into phosphosilicate glass (PSG) which is a polar material and results in device instabilities under abias-temperature stress (BTS) measurements. To limit the polarization effect, a new thin PSG process has been developed. The interface trap density of 4H-SiC-MOS capacitors using this process is as low as $3x10^{11}cm^{-2}$ eV^{-1}. BTS results on MOSFETs have shown that the thin PSG devices are as stable as NO passivated devices with mobility around 80 cm^2/V.s.

Introduction: SiC exists in different polytypes. 4H-SiC polytype has the highest bandgap energy. It has higher and more isotropic mobility compared to other polytypes and hence is used to fabricate MOSFETs [1]. To use SiC to its full potential, we must continue to work to improve the electrical characteristics of the SiO_2/4H-SiC interface by developing more efficient processes to passivate defects at the interface that form during the oxidation process [2,3,4,5]. These defects trap carriers (electrons) from the channel to become charged, thereafter acting as Coulomb scattering centres that scatter other channel electrons. The result of trapping and scattering is lower effective channel mobility [6]. At present there is a standard passivation process based on post-oxidation annealing in nitric oxide (NO) or nitric oxide followed by hydrogen annealing ($NO+H_2$) [7,8]. These passivations increase the inversion electron channel mobility of a SiC-MOSFET from single digits (~ 8cm^2/V·s) to around 35cm^2/V·s. Although these processes have made the commercialization of SiC MOSFETs a reality, there is still room for significant improvement. This inversion channel mobility value is only around 5% of bulk mobility value of SiC. In case of Si, the inversion channel mobility can be as much as 50% of bulk mobility [9]. Remember that both Si and SiC have similar bulk mobilities of around 900-1100cm^2/V·s.

Phosphorus passivation (P-passivation) is more effective for reducing the interface tarp density at the SiO_2/4H-SiC interfaces compared to NO passivation. The peak value of the effective mobility for a 4H-MOSFET after phosphorus passivation is ~ 90cm^2/V.s [10,11]. But phosphorus process causes voltage instability in the device by converting SiO_2 to phosphosilicate glass (PSG) which is a polar material [11]. The application of positive gate bias produces a sheet of positive polarization at the interface that acts in much the same way as do Na^+ atoms at the interface [12]. Our research work involved the stabilization of P-passivated devices. We showed that if a thin PSG layer capped with deposited oxide is used as the gate oxide we can stabilize the device and also keep the passivating effect of phosphorus process. We obtained a peak field effect mobility of 80cm^2/V.s using this approach.

Experiment: Silicon carbide wafers were provided by Dow Corning and Cree, Inc. MOS capacitors were fabricated on n/n+, 8^o off-axis, 4H- wafers with a 5µm n-epilayers doped with nitrogen at

$8.3x10^{15}cm^{-3}$. All the samples were cleaned prior to processing using a standard RCA process [13]. Dry thermal oxides were grown at 1150^oC (~ 6nm) and passivated with phosphorous, after 275nm, high purity molybdenum gate contacts were sputter deposited. Broad area backside contacts were formed using silver colloidal paste after backside oxide removal. High-low (1MHz/quasi-static) capacitance-voltage (C-V) measurements were used at room temperature (23^oC) to determine the interface trap density in the top-half of the 4H-SiC band gap.

Planar MOSFETs were fabricated on a 4^o off-axis 5µm p-epilayer grown on an n^+ substrate. The epilayer was doped with Al at $8x10^{15}cm^{-3}$. The gate length was 120µm. Length and width of source and drain were 200µm and 400µm, respectively.

Depending upon the thickness of the PSG layer, devices hereafter are called as thick and thin PSG devices. For a thick PSG device the layer thickness is 90nm while it is 10nm for a thin PSG device. In thin PSG device a thin layer of thermal oxide was grown and then passivated by a 2hr phosphorus passivation process [11]. The thin PSG layer was capped with a tetraethylorthosilicate (TEOS) deposited oxide (~ 45nm). The TEOS deposition was performed using an in-house LPCVD system by cracking TEOS at 650^oC and 0.6Torr. During phosphorus passivation the following reaction takes place and which leads to the formation of phosphorous pent-oxide [11].

$$SiP_2O_7 + 1000C \rightarrow SiO_2 + P_2O_5$$

Thin PSG experiment involves the following steps:

1. Thermal oxidation to get ~ 6nm of SiO_2 layer.
2. P-passivation of the interface for 2 hours.
3. Deposit ~ 45nm of SiO_2.
4. Densify the deposited oxide at 850^oC for two hours.

Results and discussion: The results of a high-low (1MHz/quasi-static) C-V measurement for a thin MOS-C are shown in Fig. 1. The corresponding interface trap density is shown in Fig. 2 and compared to results for thick PSG and NO devices. D_{it} value for thin PSG MOS device is $3x10^{11}eV^{-1}cm^{-2}$ at 0.2eV below the conduction band edge of 4H-SiC, which is two times lower than NO passivated device.

Positive BTS results for thin PSG MOS caps and MOSFETs are shown in Figures 3(a) and 3(b), respectively. Positive biases for an oxide field of 1.5MV/cm were applied at 150^oC for all samples. A different capacitor was subjected to bias-temperature stressing for each of the BTS times indicated in Fig. 3(a). The positive shift for V_{fb} in the BTS measurements of MOS capacitors is due to the electron injection and is a well-known phenomenon in NO passivated devices [14]. The thin PSG devices show much improved stability in flatband voltage (V_{fb}). Fig. 3(b) shows mobility results before and after positive BTS for 8 hours. And as we can see, there is only slight right shift (possibly due to electron injection) in the mobility curve.

The stability of thin PSG devices is due to less polarization. For a given BTS voltage, there is a direct dependence of the shift in flatband voltage on the thickness of the PSG layer [15]

$$\Delta V_{fb} = V_{fb}^{\ final} - V_{fb}^{\ initial} = Q_p / C_g = Q_p X_g / \varepsilon K_g = - \frac{K_o X_g \chi_p V_p}{K_g [(K_g + \chi_p) X_o + K_o X_g}$$

Q_p = polarization charge, C_g = capacitance of PSG layer, X_g = thickness of PSG layer, X_o = thickness of deposited oxide layer, K_g = dielectric constant of PSG layer, K_o = dielectric of deposited oxide, ε_o = permittivity of deposited oxide, χ_p = polarizability of PSG layer and, V_p = voltage during BTS.

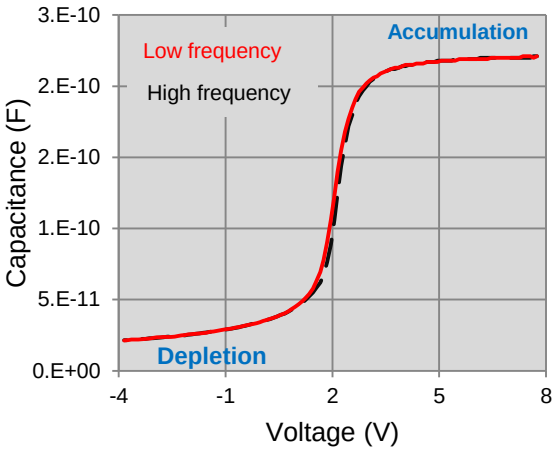

Figure 1. C-V characteristics of thin PSG MOS capacitor.

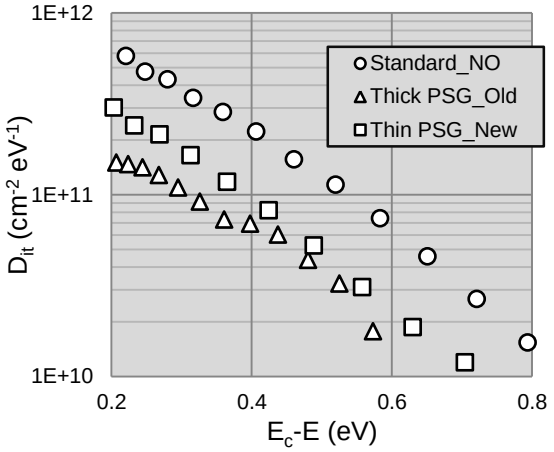

Figure 2. D_{it} for thin PSG MOS capacitor. D_{it} is lower than NO device, but higher than thick (~90nm) PSG device.

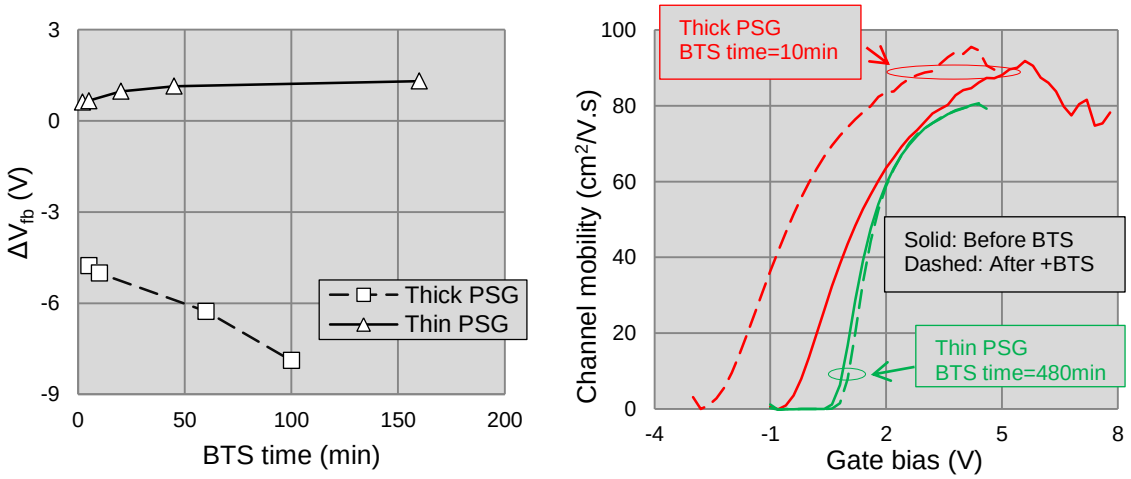

Figure 3. Positive BTS (T=150^{o}C, E_{ox}=1.5MV/cm) results for thick and thin PSG devices. (a) Flatband voltage shifts (ΔV_{fb}) for MOS capacitors. (b) Effects on mobility and threshold voltage of MOSFETs.

We see from above expression that for finite bias (V_p), ΔV_{fb} decreases with decreasing X_p. By reducing the thickness of PSG layer to 10-12nm, device stability is improved and the advantage of higher mobility compared to NO is maintained. There must be a minimum thickness of the PSG layer to keep the passivation effect of P on the interface traps**.**

Summary: To summarize briefly, by reducing the thickness of the PSG layer we can stabilize the device and at the same time do not lose the beneficial effect of phosphorus passivation. We need BTS measurements at higher temperatures (higher than 150^{o}C), higher electric fields (higher than 1.5MV/cm) and for longer time intervals to compare the stability of thin PSG devices with the stability of NO devices.

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