Deliverable A –

Review of published work and establishment of representative model and scenarios for DC fault studies

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Contents

Introduction

This document as part of *Top and Tail* work package *1.3.3 Topology, modularity and contingency* provides an initial report into protection strategies for future multi-terminal HVDC grids. At the time of writing the technology underpinning these protection strategies can be defined into two types converter based and DC breaker based. This report focuses on converter based strategies, i.e. AC/DC converters that have inherent DC fault blocking capability and do not require an additional HVDC rated circuit breaker.

The report is broken up into two sections a review of published work, detailing proposed AC/DC converter topologies for HVDC grids. Each topology is briefly summarised providing a description of its merits with particular regard to fault tolerance. The second section looks at modelling of DC grids and possible fault scenarios.

Review of Published Work

Voltage Source Converter (VSC) topologies

This section contains a literature review of proposed VSC topologies for HVDC systems. Discussion is provided on the advantages and disadvantages of each topology for HVDC power transmission and the ability of each converter to withstand DC faults. Arguments are presented based on comparison of VSC topologies and not on the comparison with line commutated alternatives.

Two level converter topology

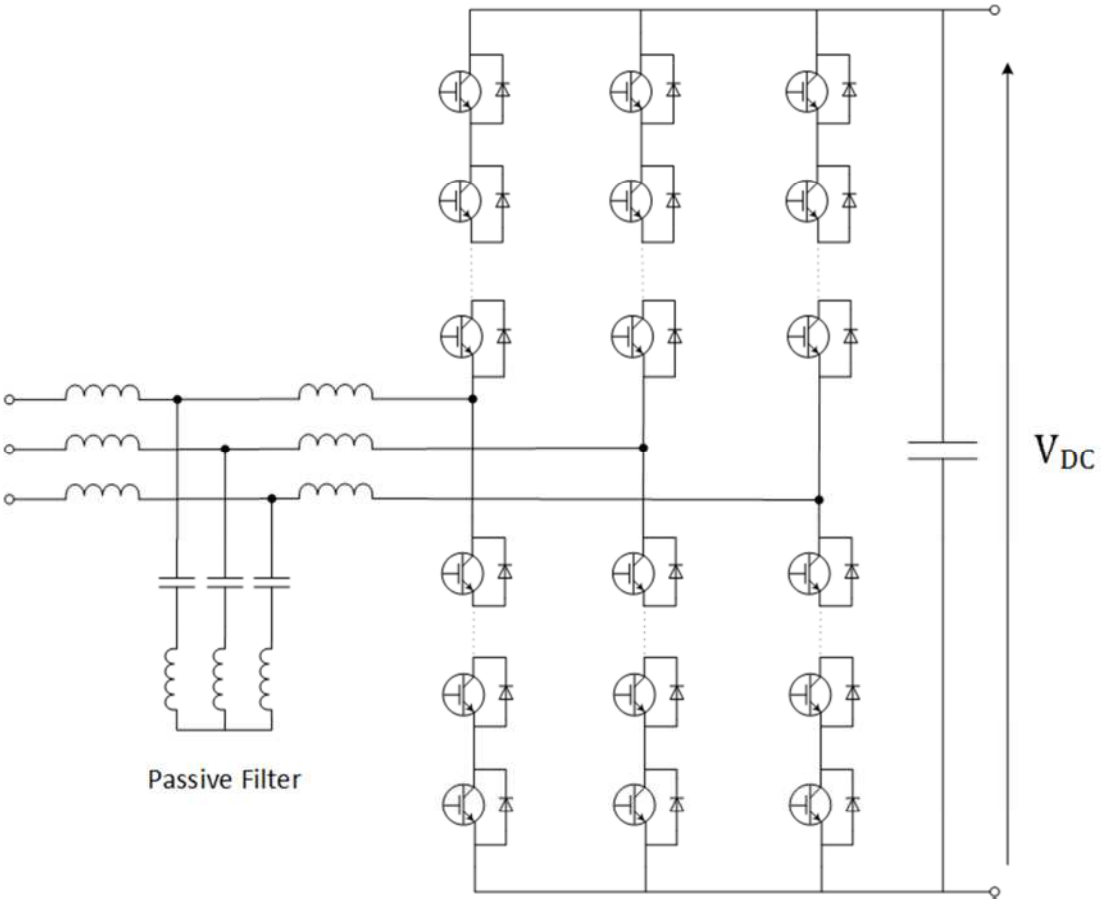


Figure 1 : two level voltage source converter [1]

In Figure 1, a two level converter is shown; for HVDC applications a high number (greater than 100) of series connected IGBTs are required to be connected in series to achieve the necessary voltage rating. The advantage of the two-level VSC for HVDC power transmission is it is a relatively simple circuit to control with techniques well published in literature [2-9]. The disadvantages of this converter when used for this application arise from the requirement to use PWM to decouple the AC voltage

from the DC voltage magnitude [10, 11]. This requires that the series string of IGBTs are hard switched introducing additional switching loss as well as extra complexity required to dynamically share the device voltage during the switching event. The PWM switching pattern will also introduce harmonics to the output voltage; which require bulky passive filters to mitigate this to acceptable levels defined by the grid code [12, 13].

Further disadvantages include poor DC side fault performance; when the DC voltage is depressed, such that the AC/DC voltage ratio exceeds that of the over-modulation region permitted by tipplen harmonic injection, then the AC voltage causes the two-level converter to rectify into DC grid and the AC breaker must be opened. Additionally when the DC grid voltage is fully reversed the IGBT diodes will begin to conduct regardless of the state of the IGBTs and the AC side breaker [14, 15].

Non-Modular Multilevel topologies

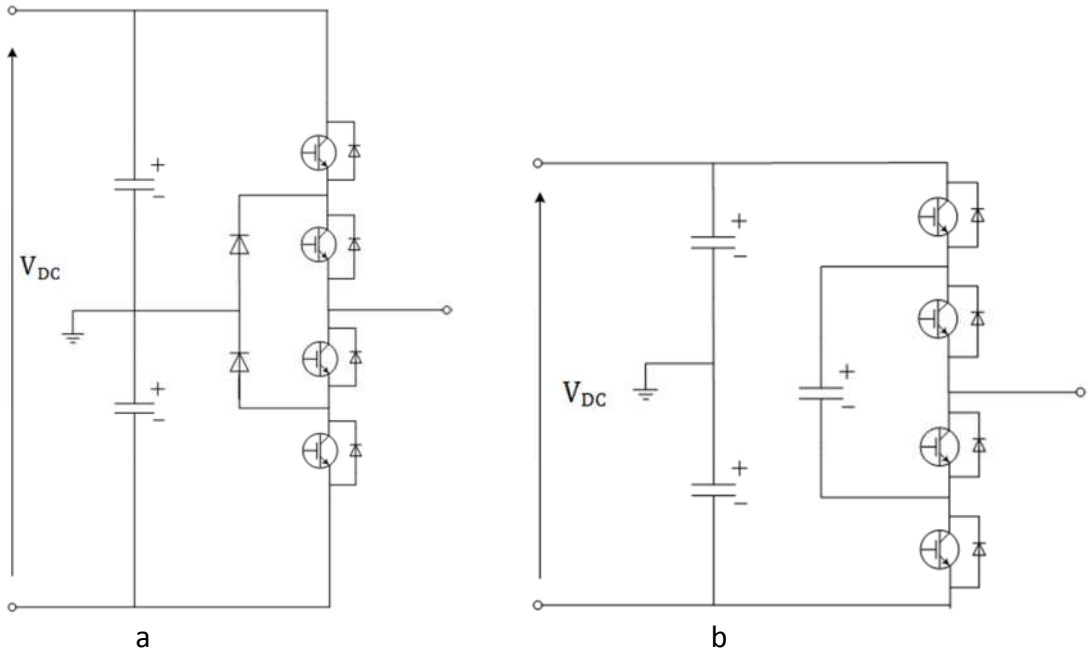


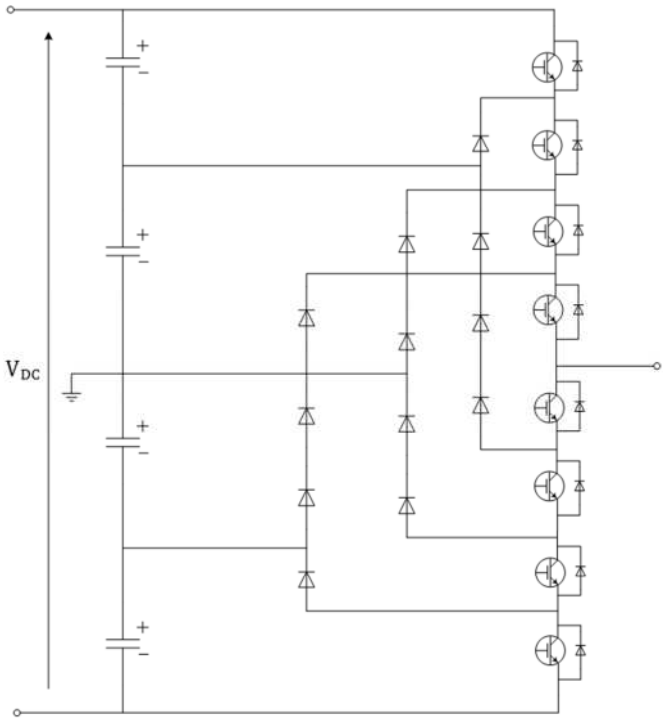
Figure 2 : a) three-level diode-clamped topology b) three-level floating capacitor topology [10]

In Figure 2 a), one phase of three-level diode-clamped converter is shown [16]. As a three-level inverter it has available voltage outputs of $+V_{dc}$, 0 and $-V_{dc}$. The advantages are relatively low switching loss and good basic AC waveform compared to the two level converter [10]. If the converter is extended to further levels additional clamping diode pairs need to be introduced as shown for the five level case in Figure 3a. The total number of diode pairs increases rapidly with the number of levels [17, 18]. For one phase of an N-level diode clamping inverter requires (N-1) capacitors, 2(N-1) switches and (N-1)(N-2) clamping diode [18]. The non-modular

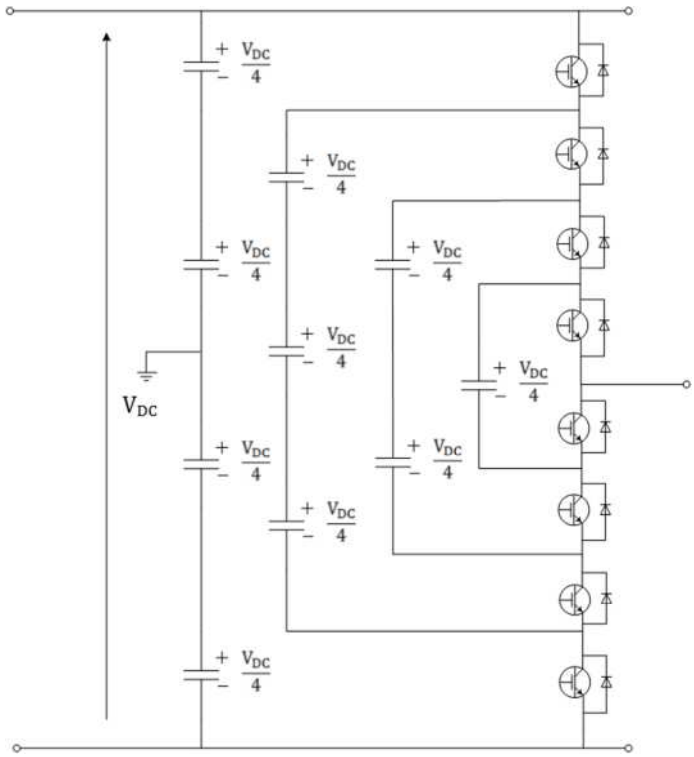
nature of the topology also means that the clamping diodes do not have a common voltage rating; i.e. some clamping diodes need to be rated for the full DC bus and others do not [19, 20]. Assuming series connected devices are used to achieve this voltage rating, it can be observed that for each extra level many more components are required. Additionally the split DC-Link capacitors introduces complexity in voltage balancing [20].

In Figure 2 b), one phase of three-level floating capacitor topology is showed. It is also called capacitor clamped and flying capacitor [21-23]. Instead of adding diode as in a), floating DC capacitor,C_f, are added. The advantages are low switching loss, good AC waveform compared to the two-level inverter. Similarly to the diode clamped-topology, when the number of levels is increased, the number of added capacitors increases rapidly, for one phase of N-level flying-capacitor converter, (N-1)(N-2)/2 flying capacitors and (N-1) main dc bus capacitors are required [19]. This large number of capacitors also leads to a large footprint [10].

As with the two-level voltage source inverter a reversal of the DC bus causes the diodes in both the diode-camped and floating capacitor topology to conduct, thus it is not suitable for use in multi-terminal HVDC systems relying on the converter to provide the fault blocking capability.



a



b

Figure 3 : (a) five-level Diode-Clamped Converter, (b) five-level floating capacitor converter

Modular multilevel converter (MMC) converter

Modular multilevel converter was first proposed in 2003 [24]. The MMC converter shown in Figure 4 (half-bridge variant shown) is constructed from a number of series connected sub-modules [1, 25, 26]. The advantages of this topology include scalability, modularity, and low switching losses [27-29].

The modular nature of the converter means that the same building blocks can be used to expand the converter to higher voltages with more levels. This has benefits for commercialization such as reducing development costs and reduction in spares holding requirements [27, 30].

Each sub-module, used as a power electronics building block, includes a self-contained DC-Link which allows at least a two-level output and at the same time restricts the voltage seen across the semiconductors. The consequence of this is that the required high voltage rating can be achieved, while semiconductor voltage sharing issues are mitigated, switching losses are reduced. Additionally the high number or output levels means the converter is able to produce a cleaner output voltage reducing passive filter requirements [31-34].

The disadvantage, of what is essentially taking the bulk energy storage components

and distributing them in a smart way around the converter, is that additionally complexity is required in the way that energy is managed [35-42].

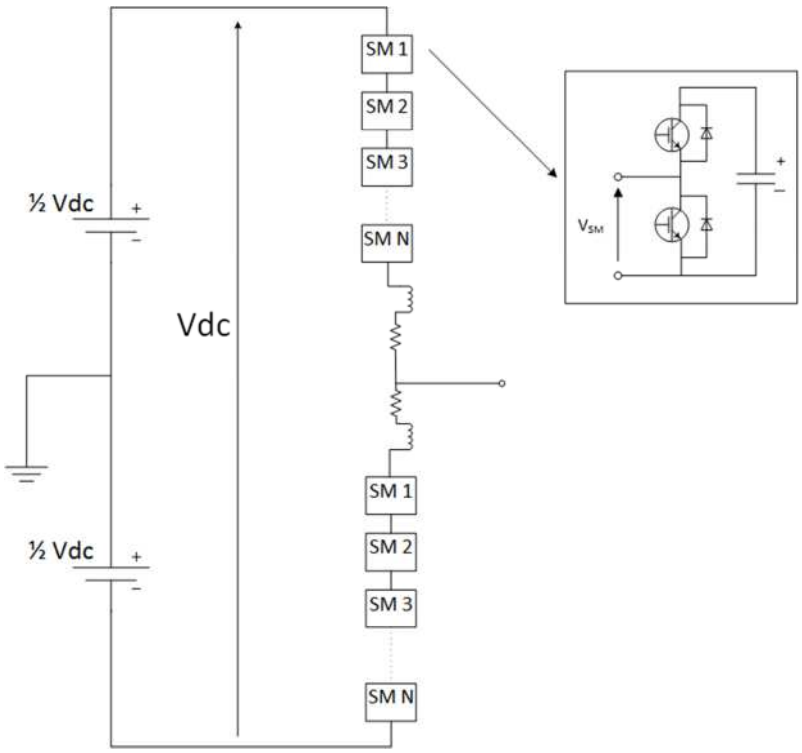
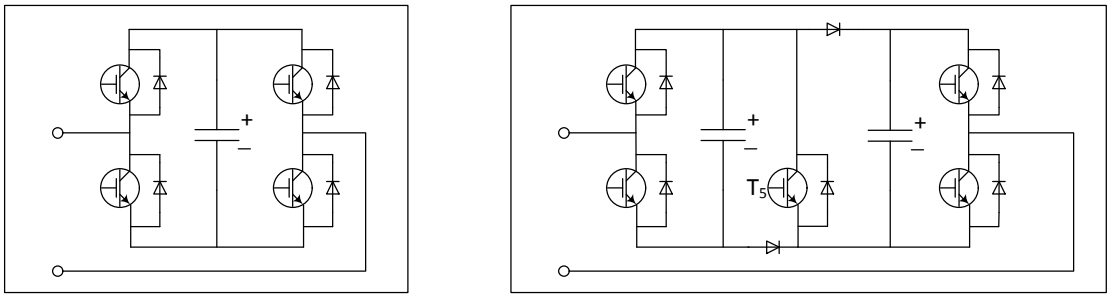


Figure 4 : One phase of MMC with half-bridge sub-module [24]

The MMC classically proposed is formed from half-bridge sub-module as shown in Figure 4. The half-bridge sub-module MMC suffers from poor fault performance for similar reasons to the two-level inverter; the IGBT anti parallel diode starts to conduct if the DC bus voltage is reversed. Additionally as each sub-module cannot produce a negative output, over-modulation is only possible via triple harmonic injection, as a consequence a DC voltage depression limits the output AC voltage such that converter will need to be disconnected via opening of the AC circuit breaker .



Full-Bridge Submodule

Clamp double submodule

Figure 5 : sub-module of Full-Bridge and Clamp-Double [25] [26]

Variants of the traditional MMC can be constructed using alternative sub-modules. Figure 5 shows proposed sub-module topologies [25]. The full-bridge sub-module is able to an output produce voltage of $+V_c$, 0 and $-V_c$. The ability to be able to produce a negative voltage means that converter is able operate up even during a full reversal of the DC bus voltage [26]. However, the use of additional semiconductors increases the losses. For Clamp-Double Sub-Module, it acts as two half-bridge sub-modules in normal condition. When the fault occurs, the IGBT T5 is able to cut off the fault current. Modular High Frequency is used for low power range.

Series Bridge Converter

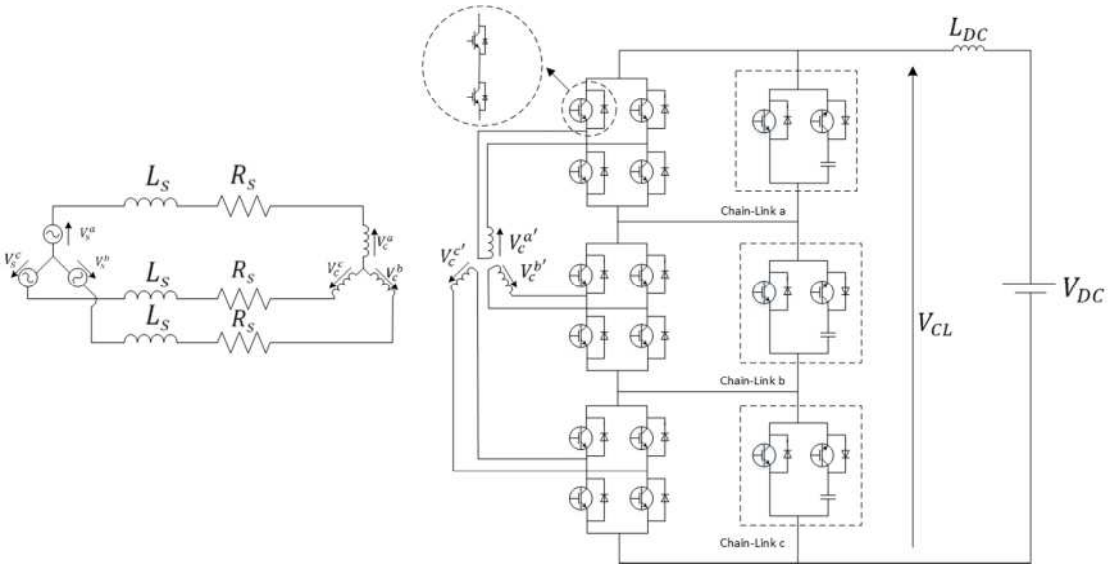


Figure 6: three phase hybrid VSC topology [43]

Figure 6 shows the VSC, referred to here as The Series Bridge Converter (SBC), first published in [43]. Each phase of the converter is constructed form an H-bridge in parallel with half-bridge sub-modules. The series-string of half-bridges are operated as to produce the rectified target AC voltage, this waveform is then “unfolded” using the H-Bridge valves which are soft switched at fundamental frequency. On the DC side, the three phases are connected in series such that rectified phase voltage sums. The addition of triplen harmonics can be used to decouple AC and DC side voltage to avoid PWM of the H-Bridge valve which sits in the main power path [43, 44]. The summation of the rectified sinusoids results in 6n harmonics on the DC bus, further injection of triplen harmonics can be used to eliminate these harmonics [45]. This technique has been extended in [46] to produce a smooth DC output voltage.

The advantages of this topology are that the loss is very low, between 0.85 to 1.2% [44, 47], and reduced sub-module size and number.

The IGBT reverse blocking diodes in both the sub-modules and the H-Bridge mean DC-Link voltage reversal will result in the conduction of these devices. Additionally

the published triplen harmonic injection technique that allows decoupling of the AC and DC side magnitudes has a maximum range that would be exceeded in DC voltage depressions.

Two level inverter with Multi-Level Series Active Filter

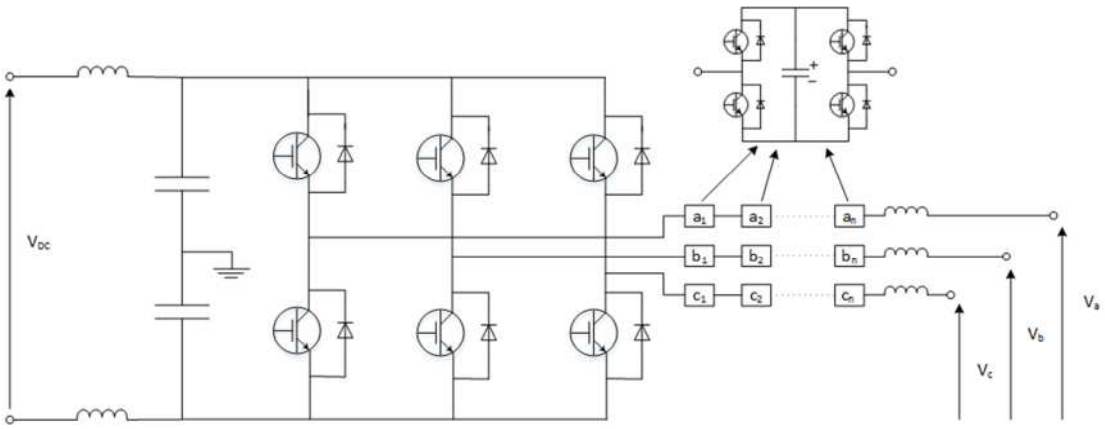


Figure 7 : Hybrid converter topology [48]

The topology depicted in Figure 7 : Hybrid converter topology [48] was first proposed for HVDC applications in [49] and further published in [48, 50].
The converter is operated by low frequency hard switching of the inverter IGBTs. The output is then actively filtered using full-bridge sub-modules [48, 50].
Advantages of this topology include, AC fault ride through, both symmetrical and asymmetrical ac faults [48, 50], it has been proposed in literature that a smaller size sub-module capacitance could be used than in the MMC [48].
The inclusion of AC full bridge sub-modules allow DC fault ride through of depressed DC bus voltages without conduction of the two level inverter anti-parallel didoes [48, 50]. In the case of negative DC voltages the inverter diodes still begin to conduct for the duration of the negative fault. However unlike a standard 2-level inverter the full bridge modules allow the AC network to be decouple from the DC fault.

Alternate Arm Converter (AAC)

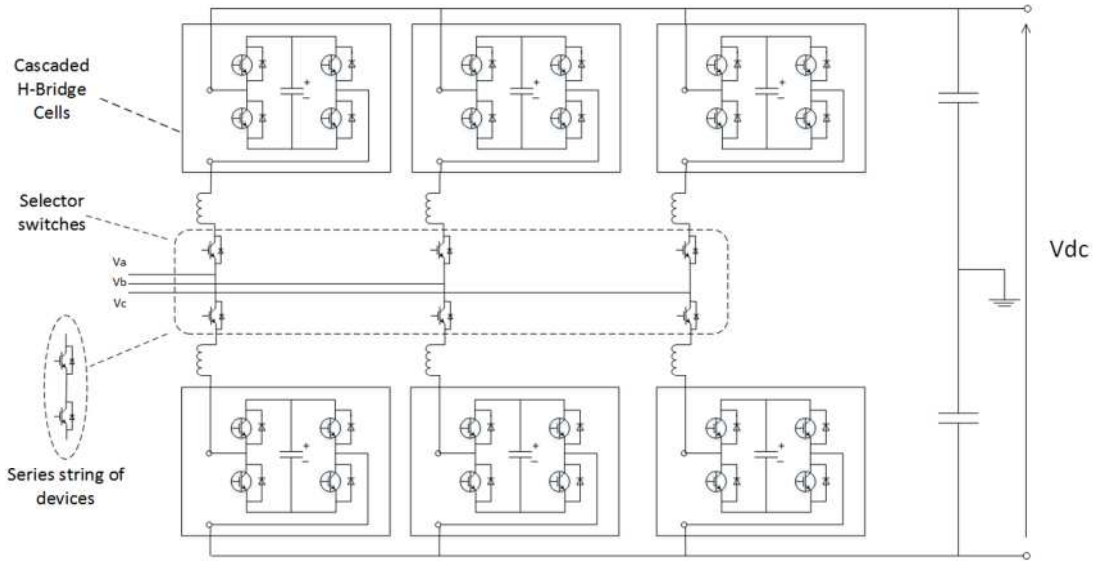


Figure 8 : Alternate-Arm Multilevel converter topology

The Alternate-Arm Multilevel converter (AAC) first proposed in [49] and more extensively published in [51-56], is depicted in Figure 8. In this hybrid topology, a series string of IGBTs are connected in series with a series string of full-bridges sub-module to form a converter arm. The addition of the series string of IGBTs, referred to as a director switch, enables the arm to be switched off for approximately half of a fundamental period. Doing so allows the positive and negative half cycles to be generated by upper and lower arm respectively, such that the arm available voltage requirement is approximately halved with respect to the MMC, thus the number of sub-modules required is reduced [53].

The action of switching each arm in and out at fundamental frequency has the effect of rectifying current into the DC-Link such that a DC filter is required to prevent un-wanted DC current harmonics [51, 53]. Additionally the circuit must be operated around a ‘sweet spot’ for optimal performance [53]. This sweet spot voltage requires the converter to over-modulate such that full-bridge sub-modules are required. The use of full-bridge sub-modules gives the circuit inherent DC fault blocking capability and allows it operate during DC faults [51].

Establishment of Representative Model and Scenarios for DC fault studies

In this section physical properties of DC grids are considered such as converter arrangement and cable layout, this is conducted in order that the HVDC grids can be correctly modelled and additionally likely fault scenarios established.

Converter layout

The arrangement of VSCs converters for HVDC power transmission can be classified into the following types, asymmetric monopole, symmetric monopole and bipole. Here a brief description of each type of system is presented.

Asymmetric monopole

Asymmetric monopoles feature a single HVDC converter connected via a single conductor at the full HVDC voltage. A return path for the current is made via ground connection or a metallic return. The advantage of earth return is reduced cable investment cost and transmission loss compare to metallic return; however, continuous flow of current through earth is not always permitted in which case a metallic return must be provided [57].

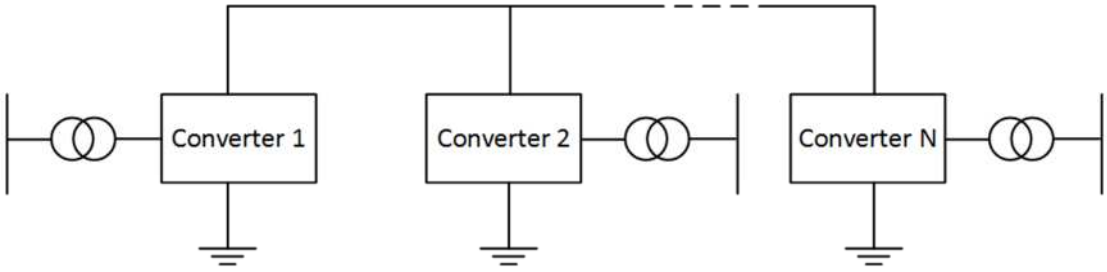


Figure 9 a monopole HVDC grid with earth return [58]

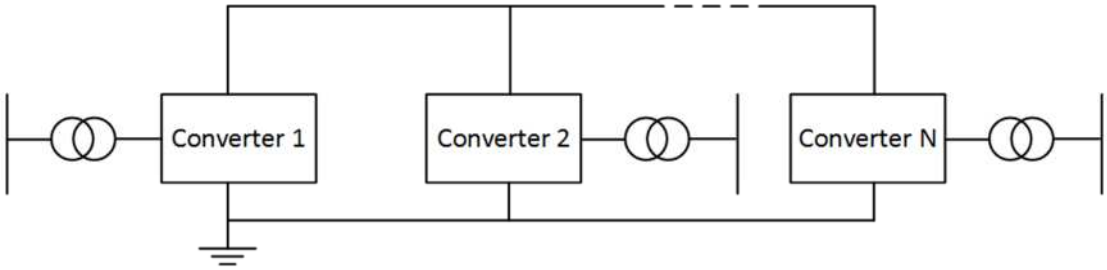


Figure 10 a monopole HVDC Grid with metallic return [58]

Symmetric monopole

Symmetric monopoles feature a single HVDC converter connected via two conductors. The converter is earthed such that there is equal potential between the upper and lower terminals and ground. In normal operation, no current flows through the earth [58].

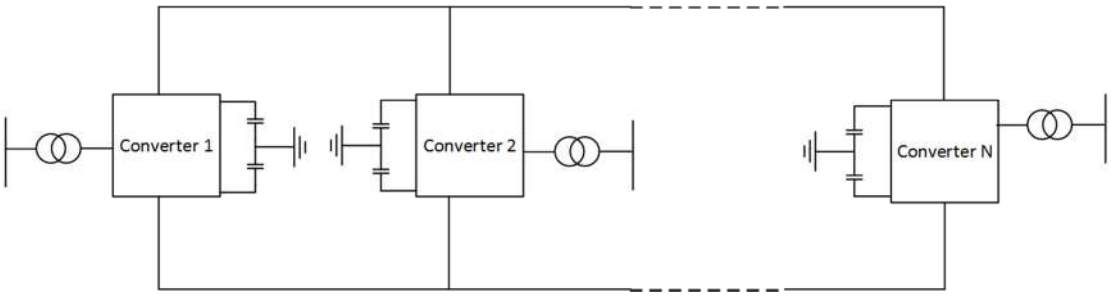


Figure 11 Symmetrical monopole configuration [58]

Bipole

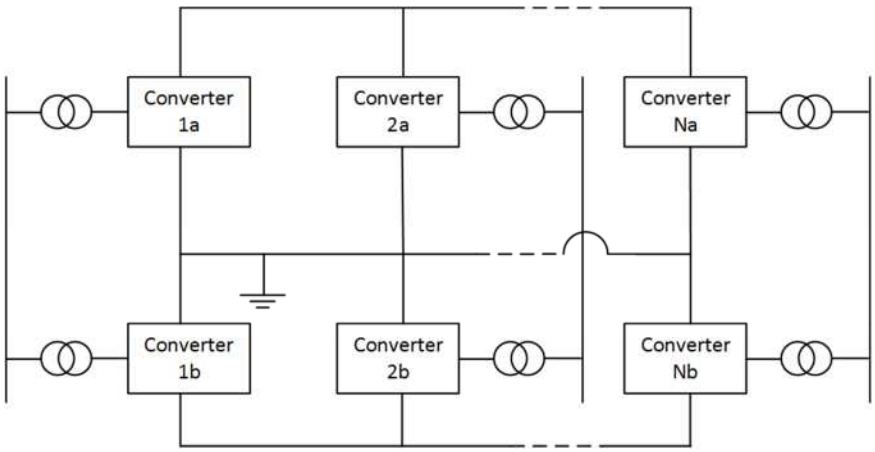


Figure 12 a bipolar HVDC Grid with dedicated metallic return conductor [58]

A bipole consists of two HVDC converters connected in series with a ground connection in the middle. The DC-link is connected to a bi-pole grid via two conductors.

HVDC cable

HVDC cables systems include three parts: cable, joint and end terminations. The joint is used to connect cables to reach the desired length. The end termination is used to reduce the electrical stress at the end of the cable to provide adequate electrical and mechanical properties [59]. Presently there are mainly two types of cable used for HVDC VSC systems: Mass-impregnated HVDC cables and Extruded HVDC Cable such as XLPE (self-contained fluid filled SCFF is also available, but not widely in use) [60, 61].

Mass-impregnated (MI) cable is also known as paper lapped cable. Figure 13 shows the structure of Mass-Impregnated cable. It uses the paper tapes as the insulation [59, 62]. Currently this type of cable is mostly used because they have been in service for 40 years and highly reliable. At present the rating is up to +/- 600kV and 1800 A DC [63]. The conductor size is typically up to 2500mm^2.

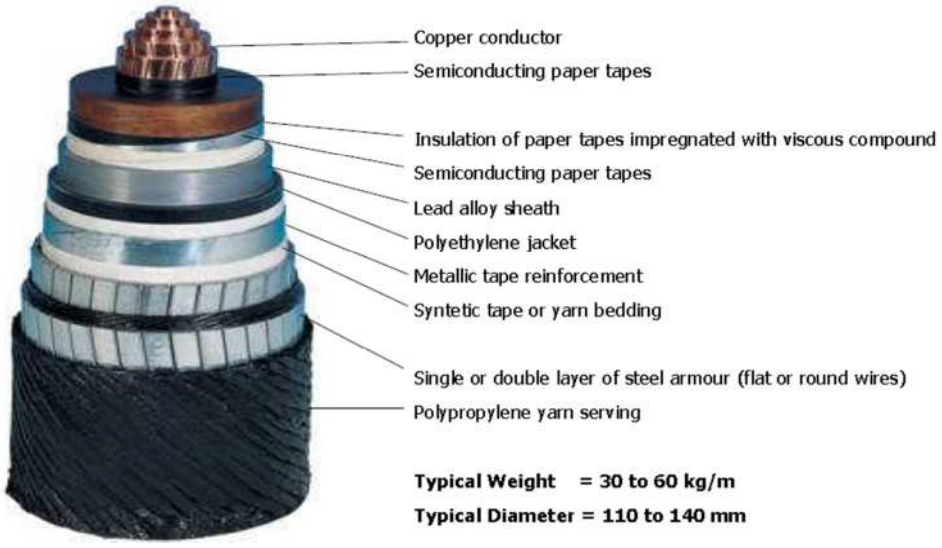


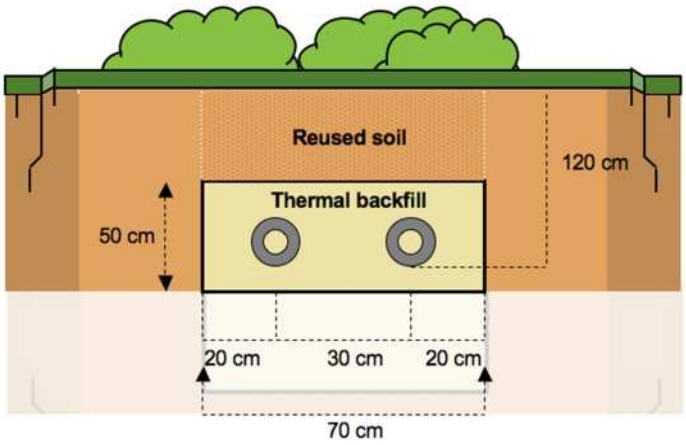
Figure 13 the structure of Mass-impregnated (MI) cable [64]

Extruded cable is also known as polymeric cable. Figure 14 shows the structure of extruded cable. Extruded cables such as Cross-Linked Polyethylene (XLPE) cables are mainly used in Voltage Source Converters applications that allow the power flow to reverse without reversing the polarity [62, 65]. To date, this technology has been applied at voltages up to +/- 320 kV (in service with a power capacity of 800 MW) [66], and up to 525 kV, 2.6 GW extruded HVDC cable system has been developed

[67].

Figure 14 structure of extruded cable [64]

Where HVDC cables are buried underground the cables are buried usually 1-1.5 meter deep and 1 meter wide. As shown in Figure 15 [60].
There are several ways to install the HVDC cables. Typically, HVDC cables are buried underground 1-1.6 meter deep and 1 meter wide. As shown in Figure 15 upper: 1 Bipole HVDC system, 320kV, 1 GW lower: 2 Bipole HVDC system, 320kV, 2 GW [60] [60]



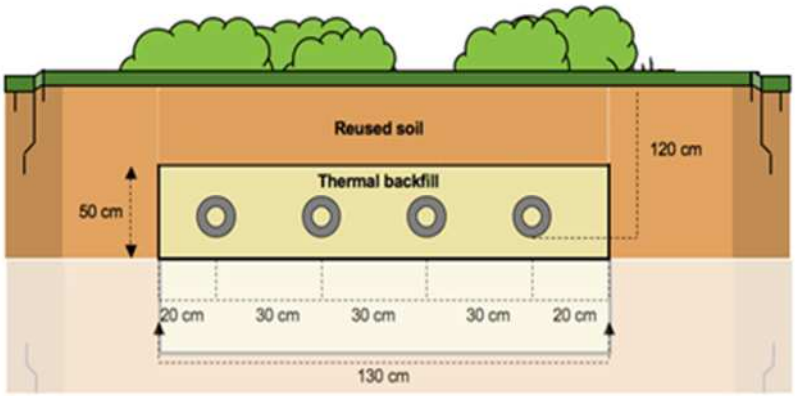


Figure 15 upper: 1 Bipole HVDC system, 320kV, 1 GW lower: 2 Bipole HVDC system, 320kV, 2 GW [60]

In submarine cable installations a distinction is made between shallow water cable lying (i.e. up to a maximum depth of 500m) and deep water cable lying (i.e. a depth from 500m up to 2.000m). For cable systems in shallow waters, burial is mandatory to protect the cable against the risk of damage from fishing gear and anchors [68-70]. The cable can be buried in bundle configuration (as shown in Figure 16) or individually. When buried individually, the distance between the cables will be at least the water depth (Figure 17). In deep water, the threat of anchors is no longer exist, so a burial operation can be omitted. The distance between the cables is usually as great as twice the sea depth. As shown in Figure 18. The purpose of the large distance is avoiding overlapping when recover the cable from damage [63, 68].

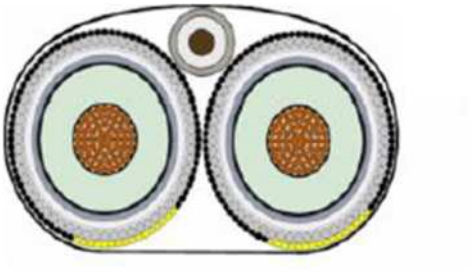


Figure 16 : two power and one optical cable in a bundle configuration (used in The Trans Bay San Francisco Interconnection)

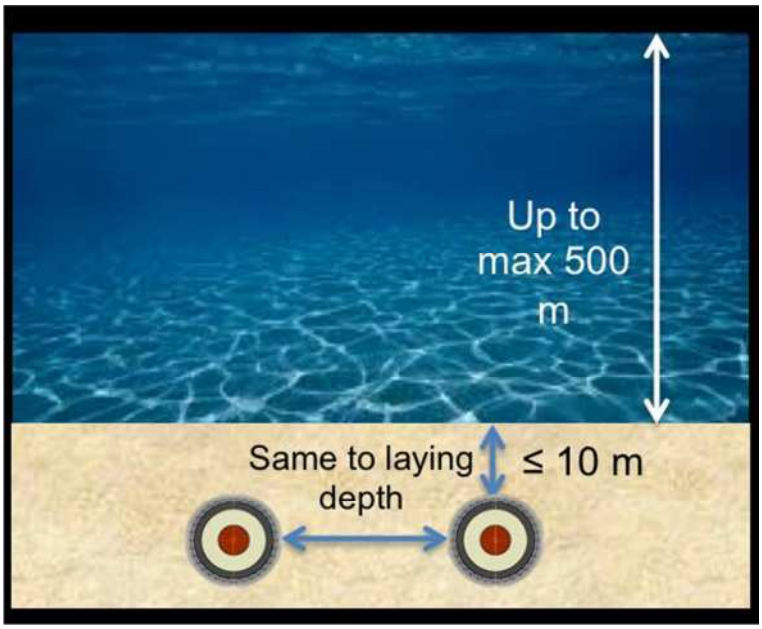


Figure 17 submarine cable laying in shallow water [63]

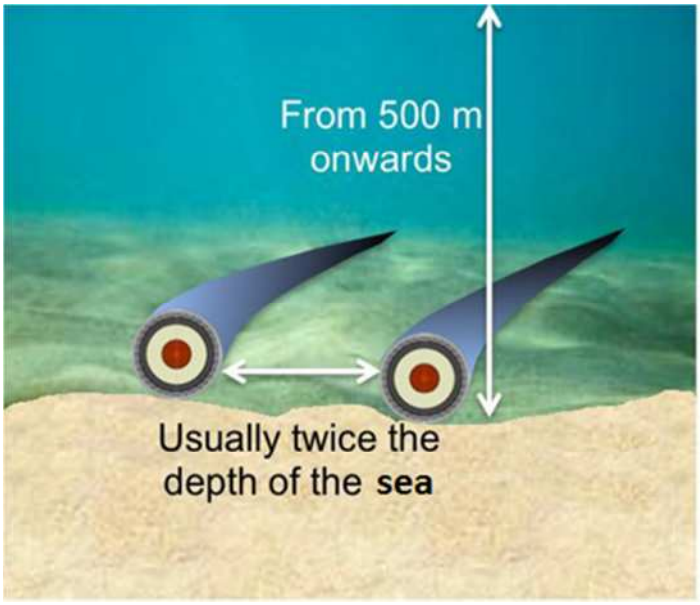


Figure 18 Submarine cable laying in deep water [63]

Cable Modeling

Here the published techniques of cable/line
There are already several overhead line or

PI section model

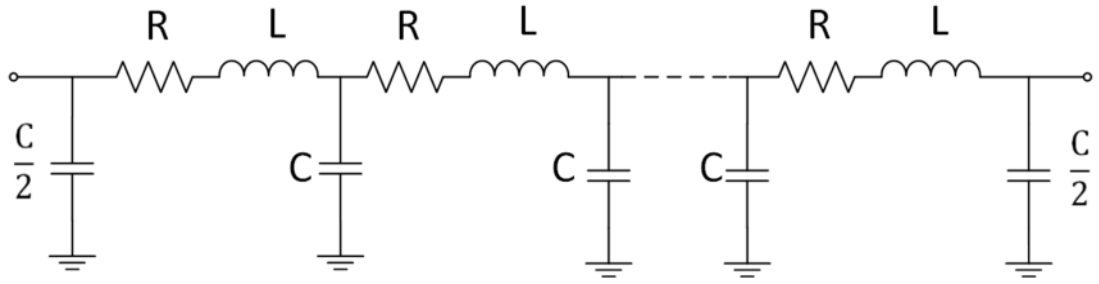


Figure 19 : the configuration of PI model

PI section model represent the

The required number of sections for the distributed parameter model is a function of frequency of interest and cable length. An equation for calculating the required

$fmax=N·v8ltotal$ (1)**Error! Reference source not found.**.

$$f_{max} = \frac{N \cdot v}{8 l_{total}} \quad (1)$$

Where f_{max} is the approximation of the maximum frequency range represented by PI line model, *N* is the number of PI sections, v is the propagation speed, l_{total} is the length of the line.

The result of this relationship means that as the cable length increases, for a given frequency of interest, the required number of sections makes the model cumbersome. Additionally the insertion of discrete lumped components introduces extra resonant combinations between capacitors and inductors such that *false resonances* may be observed when using this model.

Bergeron Model

The Bergeron model represents the line inductance and capacitance as distributed parameters while the cable resistance is represented as a lumped parameter [77]. It is accurate for a certain frequency since all calculated parameters are calculated at this specific frequency. The Bergeron model is roughly equal to PI model with infinite sections, thus when the transmission line is long enough (transport delay longer than simulation time step), the Bergeron model is preferable to the PI model [74].

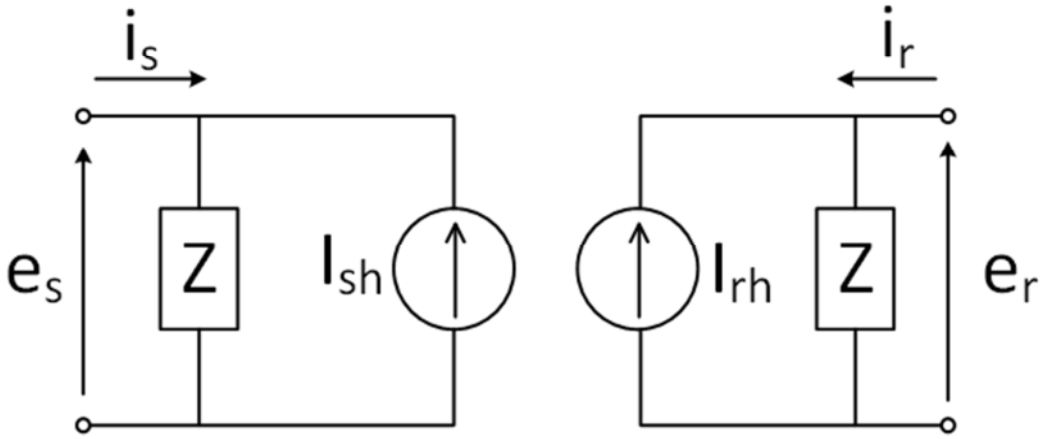


Figure 20 distributed parameter line [78]

$$I_{sh} = \left(\frac{1+h}{2}\right)\left[\frac{1}{Z}e_r(t-\tau) + hi_r(t-\tau)\right] + \left(\frac{1-h}{2}\right)\left[\frac{1}{Z}e_s(t-\tau) + hi_s(t-\tau)\right]$$

$$I_{rh} = \left(\frac{1+h}{2}\right)\left[\frac{1}{Z}e_s(t-\tau) + hi_s(t-\tau)\right] + \left(\frac{1-h}{2}\right)\left[\frac{1}{Z}e_r(t-\tau) + hi_r(t-\tau)\right]$$

Where

$$Z = Z_c + R/4$$
$$\tau = l\sqrt{L'C'}$$
$$h = \frac{Z_c - R/4}{Z_c + R/4}$$

Where Zc is the characteristic impedance, τ is the transport delay, l is the line length [77-80].

Frequency dependent model

A limitation of the Bergeron model is that the line parameters are not frequency dependent; thus, the skin effect cannot be included into the Bergeron mode. The frequency dependent model parameters are solved in frequency domain, they are then convolved into their equivalent time-domain characteristics. It represents R, L and C as distributed parameters.

Frequency dependent (phase) model is based on the theory in [81, 82]. The propagation function matrix H and the characteristic admittance matrix Y_c are calculate in frequency domain, and then approximated and replaced by equivalent low order rational functions. It is the most accurate model [83]. The time domain implementation is shown in Figure 21.

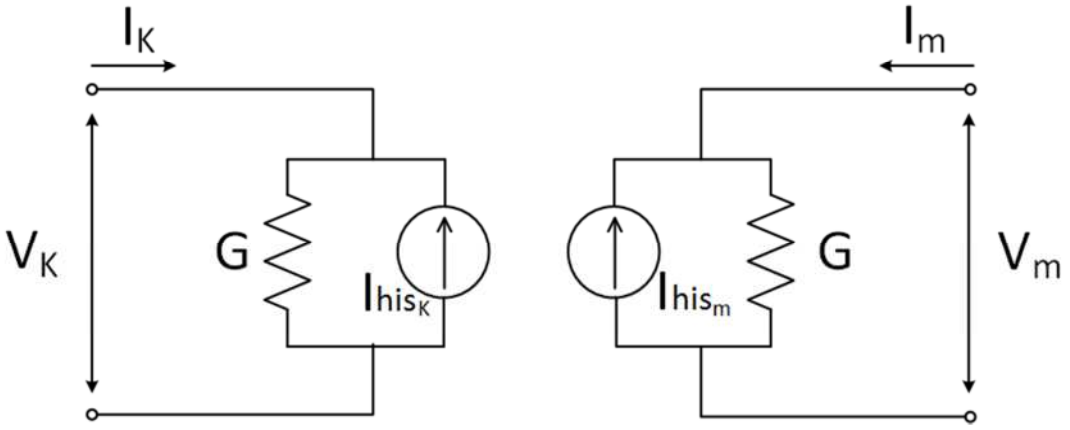


Figure 21: Norton equivalent for transmission line model [82]

$$I_k(n) = G \cdot V_k(n) - Ihis_k(n)$$
$$I_{kr}(n) = I_k(n) - I_{ki}(n)$$
$$I_{ki}(n+1) = H * I_{mr}(n-\tau)$$
$$Ihis_k(n+1) = Y_c' * V_k(n) - 2 \cdot I_{ki}(n+1)$$

Where $*$ indicates a convolution integral

$H = e^{-\sqrt{ZYl}}$, is the propagation function matrix

$Y_c = Z^{-1} \cdot \sqrt{ZY}$, is the characteristic admittance matrix

Fault Scenarios

Definitions of fault scenarios in DC grids are established in this section. Faults are divided into dual pole faults involving two conductors and single pole faults restricted to one conductor in the system.

Dual pole faults

In HVDC systems where two conductors are used it possible that both conductors become faulted, this condition is referred to here as a *dual pole fault*. Below is a list of expected dual pole faults.

Pole to Pole short – This is the direct zero impedance connection of both positive and negative conductors to each other. Where armored cable has been used it is also likely any short of the conductors would also likely mean both poles are grounded.

Pole to Pole non-zero impedance connection - The connection of both positive and negative conductors to each other via some impedance.

Dual pole open Circuit - Both conductors in the system become open circuited. Again where armored cable is used, assuming a conductive object causes the fault, it is likely the cable would be short circuited first.

Asymmetric dual pole faults – In sub-marine cable installations it is unlikely that the dual pole faults would occur from a single event, thus it can be reasoned that the fault mechanism in each pole could be different. For convenience these are lumped together here under the term asymmetric dual pole faults; in these case the faults could be any of the single pole faults listed in the following section.

Single pole faults

In HVDC systems where either a single conductor or two conductors are used the following fault scenarios are considered.

Single pole short to ground – A single conductor in the system is shorted to ground.

Single pole non-zero impedance connection to ground – A single conductor in the system is connected to ground via an impedance.

Single pole open circuit – In this scenario a single conductor in the system is open circuited. In the case of armored cable this would likely result in an initial short circuit.

Non-Zero impedance faults

Non-zero impedance faults are caused by objects providing unwanted conduction paths in the system, such that a non-zero impedance is provided between conductors or to ground. In a AC system is possible that such a fault would cause a voltage depression of the system, in a HVDC grid any non

Fault duration

In studying HVDC system faults the duration of the fault must also be considered; fault duration can be classified by its impact on each system.

Type 1 – Less than or a few fundamental periods. Faults that do not last long enough for a steady state to be reached in an electrical system.

Type 2 – Several electrical fundamental periods. Faults that are long enough for a

steady state to be reached in the electrical system but only cause thermal transients.

Type 3 – Temporary. Faults that are short enough that the system may be temporary overloaded if needed.

Type 4 – Semi-permanent. Faults that may last several days or even months. The system should be operated within the limits of the ratings.

Fault location

Where the faults occur in the system must also be considered. At the extremes this could be at the station terminals or in the case of a point to point scheme in the middle of two stations.

Conclusion

This report has provided a literature of proposed HVDC converter stations for future multi-terminal DC grids. Many converter topologies have been proposed in literature and it is evident that research is currently focused into Multi-Level VSC topologies. Of these topologies only the Two level inverter with Multi-Level Series Active Filter, fault blocking variants of the Modular Multi-Level Converter and the Alternate Arm Converter provide DC-fault blocking capability. The *Two level inverter with Multi-Level Series Active Filter* prevents DC faults propagating on to the AC network, but does not provide full DC-side fault blocking capability. The full-bridge Modular Multi-Level Converter and the Alternate Arm Converter provide full DC fault blocking capability.

A study of HVDC system components and layouts has shown the different possible arrangements for HVDC systems, the different types of cable used in HVDC systems and the different ways these can be modelled. This has allowed fault scenarios to be established and will allow a representative model of an HVDC system to be established.

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