Impact of N_2O passivation on 4H-SiC/SiO_2 interfaces grown at high-temperature

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Abstract: The authors investigated the effect of high-temperature post-oxidation nitrous oxide (N_2O) annealing on thermally grown 4H-SiC MOS capacitors. The temperatures used for oxidation are 1200^{o}C and 1500^{o}C. MOS capacitors with the 1200^{o}C oxidation process were annealed with N_2O at 1350^{o}C and 1450^{o}C, with the former temperature proved to be more effective in reducing the interface trap density (D_{it}). For the 1500^{o}C oxidation process the post-oxidation annealing is done at 1350^{o}C. Out of all these processes the 1500^{o}C thermal oxidation followed by 1350^{o}C post-oxidation N_2O annealing gives the lowest D_{it} of $3x10^{11}$ $cm^{-2}eV^{-1}$ at 0.2eV away from the conduction band (CB) edge. Although the berakdown volatge of the device is signficatly lower than 8MV/cm.

Introduction: The 4H-SiC power metal-oxide-semiconductor field-effect-transistor (MOSFET) is a good choice as a power device for operating voltages higher than 1kV. 4H-SiC MOSFETs with voltage ratings of 1.2kV and 1.7kV are now commercially available and higher voltage devices up to 21kV have been demonstrated. Due to the higher critical field of breakdown (2.2MV/cm) of 4H-SiC, seven times higher than Si, the on-state losses for are lower than their Si counterparts. For a 4H-SiC MOSFET, a good quality interface 4H-SiC/SiO_2 is very important. For a standard oxidation process (1200°C thermal oxidation), the interface is very poor, resulting in a single digit field-effect mobility. At present, in commercially available MOSFETs, after growing the interface a post oxidation annealing is done. This process is commonly known as the interface passivation process as it reduces the interface trap density (D_{it}) by passivating the traps generated after standard thermal oxidation. Currently, nitric oxide (NO) or N_2O post-oxidation annealing (interface passivation) is done at 1175^{o}C to increase the mobility up to 35cm^2/V-s [1,2]. This value is only 5% of the maximum theoretical bulk-mobility of 4H-SiC. Other interface passivations have been used to improve the interface, but all have their own limitations [3-8]. Recently, results on high-temperature oxidation (1500^{o}C) have shown a reduction in the interface trap density (D_{it}) without performing any kind of post-oxidation annealing [9,10]. However to the author's knowledge no post-oxidation N_2O annealing studies have been performed on the MOS capacitors fabricated using the high-temperature oxidation process.

Experimental: An (0001) n-type 4^o off 4H-SiC wafer was diced into 8cm x 8cm samples before organic and RCA cleaning. The wafer had a 10 µm thick n-epitaxial layer doped at $1x10^{16}/cm^3$. The samples then underwent either thermal oxidation at 1200^{o}C (flow rate 1L/min) followed by 2hr N_2O annealing at 1350^{o}C/1450^{o}C or thermal oxidation at 1500^{o}C (flow rate 0.05L/min) followed by 2hr N_2O annealing at 1350^{o}C. The details of various processing step can be seen in [9,10]. All the samples were subsequently patterned for sputter-deposited, 400nm Al gates. After removing the oxide, back-side contacts were made by sputtering Ni with the n+ substrate. High–low C–V measurements at room temperature were

made to determine the D_{it}. Current– voltage (I-V) measurements were also carried out the room temperature to examine the breakdown characteristics of the oxide.

Results and Discussion: The interface trap density for N_2O annealed MOS capacitors, grown via high-temperature oxidation (1500^{o}C) are shown in Fig. 1. There is a decrease in the D_{it} ($7x10^{11}cm^{-2}eV^{-1}$ at 0.2eV from the CB edge) for the high temperature as-oxidized MOS capacitors as compared with the MOS capacitors grown using standard oxidation process (1200^{o}C), Fig. 2(a). The high-temperature oxidation followed by N_2O annealing performed at 1350^{o}C shows an improvement in the D_{it}, with values lies in the range of $(2\text{-}6)x10^{11}cm^{-2}eV$. Fig. 1 also shows the I–V characteristics of these devices. All the devices are found to have a higher leakage current compared to typical as-oxdizied or N_2O anealed MOS capacitors leading to significatly lower oxide breakdown (~5MV/cm). The high-temperature as-oxidized MOS capacitors have breakdown voltages are better (in the range of 6.5-7.0MV/cm) as compared with annealed device but still lower than 8MV/cm. This behaviour could be due structural changes in the oxides grown at high-temperature. At such a high temperature the oxidation rate is very high as compared with the 1200^{o}C oxidation process, and which may lead to the different stoichiometry of the oxide [9], and required further in-depth physical analysis to understand this. As mentioned above we also studied the effects of annealing temperature during the post-oxidation annealing of the MOS capacitors, with gate oxides grown at 1200^{o}C. The results are shown in Fig. 2. As we can see that as-oxidized MOS capacitors gives a high D_{it}, $2x10^{12}cm^{-2}eV^{-1}$ at 0.2eV form the CB edge, with breakdown voltages of these devices around 8MV/cm. These values are consistent with the literature. Devices with 1350^{o}C N_2O annealing gives a low D_{it} of $7x10^{12}cm^{-2}eV^{-1}$, but, like annealed high-temperature MOS capacitors the breakdown voltage is less than 8MV/cm. The results for 1450^{o}C N_2O annealed devices are shown in Fig 2(c-f). As we can see there is no improvement in D_{it} with the increase of annealing temperature up to 1450^{o}C during N_2O annealing. The breakdown data for N_2O passivation at 1450^{o}C could not be obtained due to a high increase in the oxide thickness after performing N_2O annealing.

In conclusion, the effect of N_2O post-oxidation annealing is studied on the MOS capacitors fabricated with the low (1200^{o}C) and high (1400^{o}C) temperature oxidation processes. Also the effect of annealing temperature during N_2O annealing is studied on low temperature MOS capacitors. The high-temperatures MOS capacitors followed by 1350^{o}C post-oxidation N_2O annealing gives the lowest D_{it}, $(2\text{-}6)\ x10^{11}cm^{-2}eV^{-1}$. For the low temperature, N_2O annealing at 1350^{o}C is the most effective with D_{it} of $7x10^{12}cm^{-2}eV^{-1}$ at 0.2eV away from the conduction band edge. Although it has been found out that all these processes lead to lower oxide breakdown fields (<8MV/cm).

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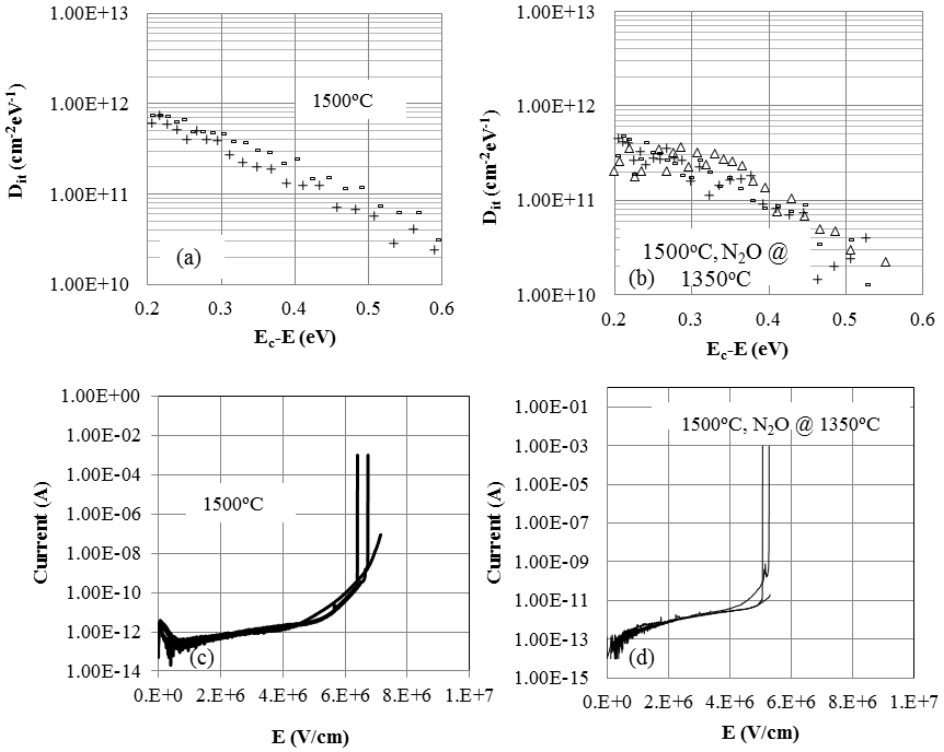

Fig. 1. Typical I-V characteristics of 4H-SiC MOS capacitors with a high-temperature (1500°C) thermal oxidation followed by with/without post-oxidation N_2O annealing at 1350°C, interface trap density (a-b), and oxide breakdown (c-d).

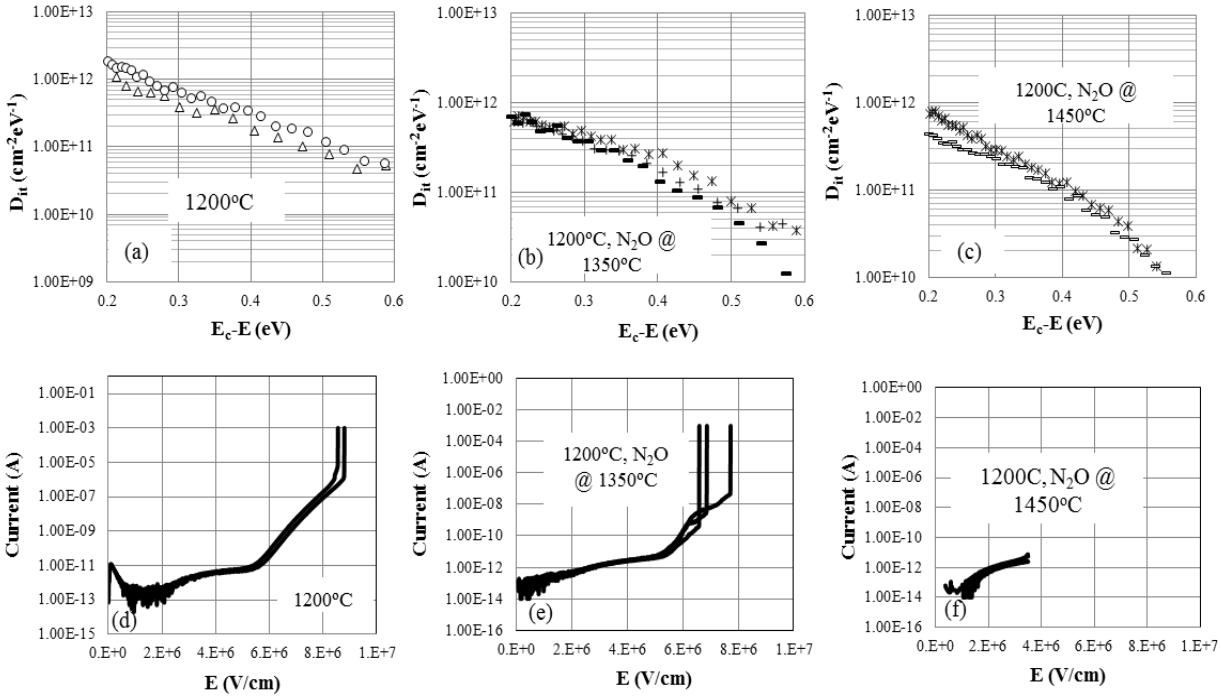

Fig. 2. Typical I-V characteristics of 4H-SiC MOS capacitors with a standard oxidtaion process (1200°C thermal oxidation) and followd by post-oxidation N_2O annealing at 1350°C and 1450°C.