High Efficiency DC-AC Converter for Low Voltage DC Distribution Networks

University of Strathclyde Engineering

Top and Tail Transformation
A Grand Challenge in Energy Networks

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1. LVDC Distribution System

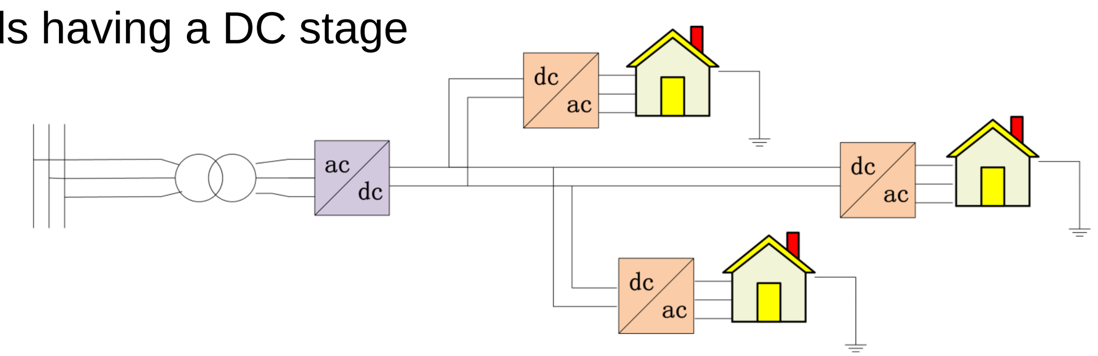
Challenges of existing distribution networks

- Increased loads
- High-capacity power electronic interfaces: embedded PV generation & EV chargers

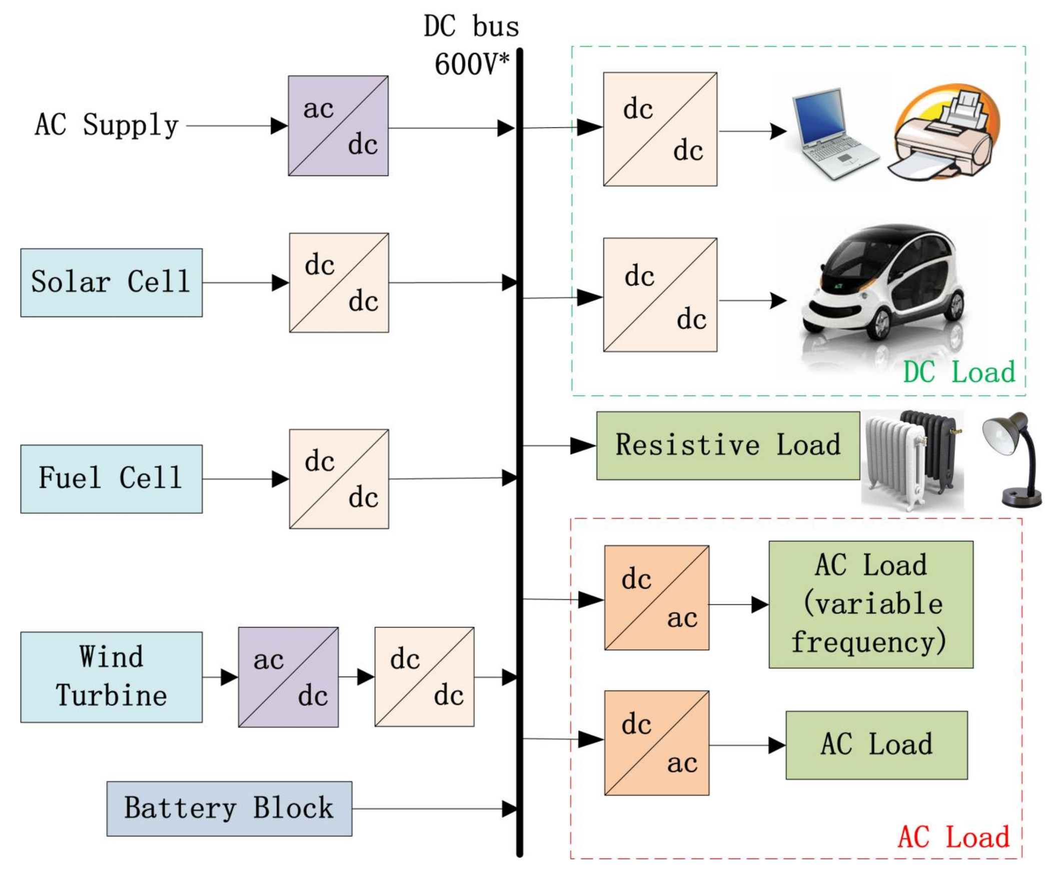
Benefits of LVDC Distribution Networks

- Larger power capacity and reduced cable losses
- No reactive power, lack of frequency stability and skin effect issues
- Better immunity to harmonic current and voltage imbalance
- The growth of power electronic loads having a DC stage

However it must accommodate existing AC loads which must be fed by local DC-AC inverters.



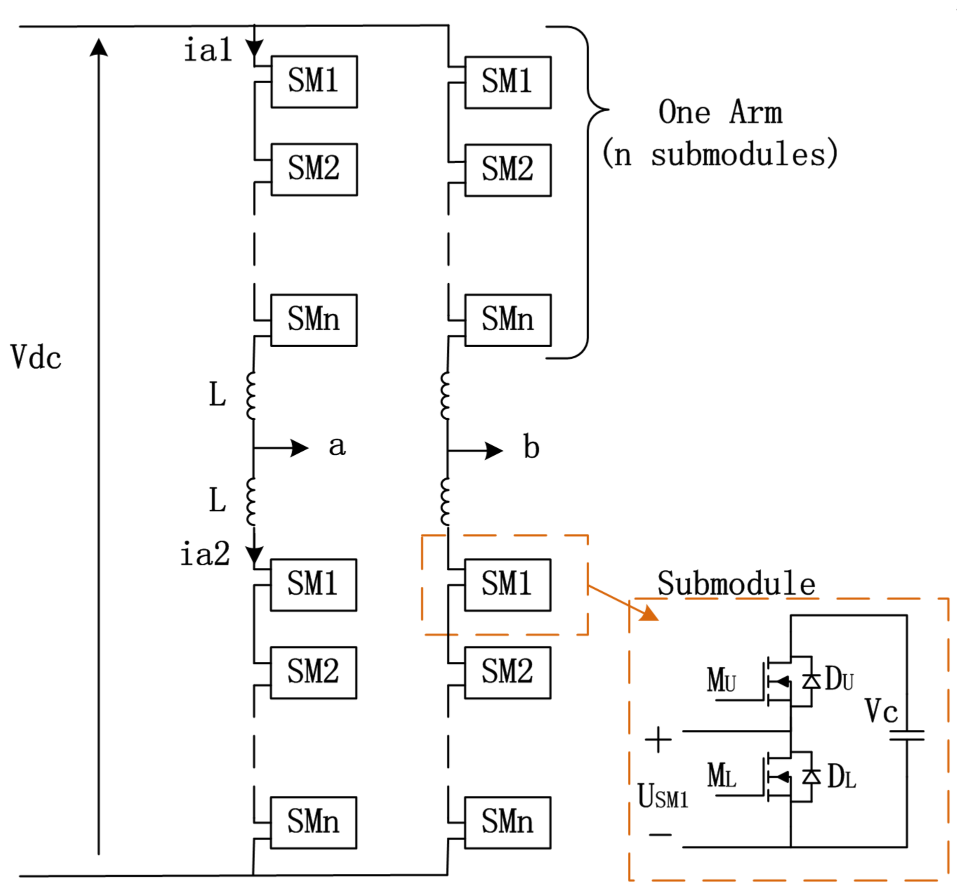
A proposed LVDC distribution network with customer-end inverters



A proposed LVDC distribution network with both DC and AC supplies inside the house

2. An Efficient DC-AC Converter for Distribution Systems (Loss Calculation)

Proposed Multilevel Converter (MMC):

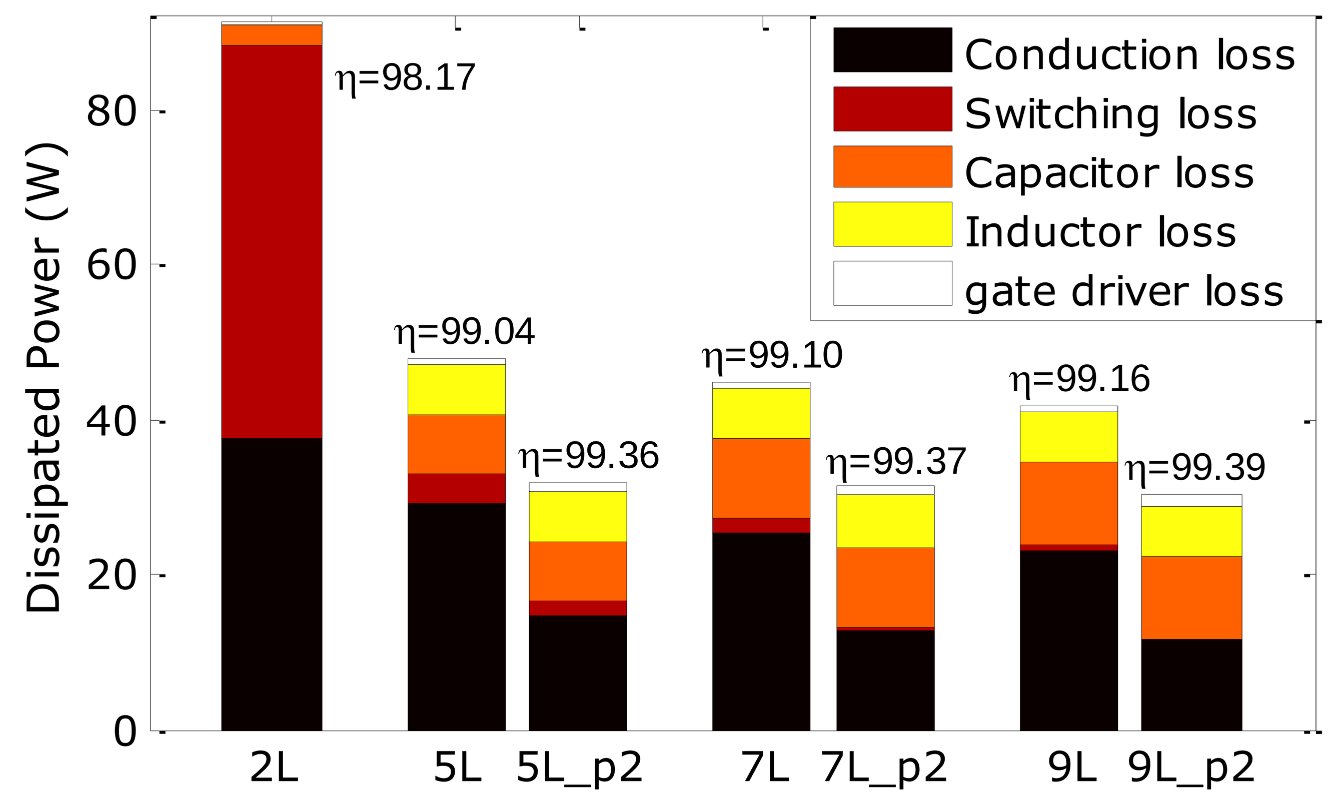


Modular Multilevel Converter(MMC)

Advantages:

- MOSFET: low on-state conduction loss
- Synchronous rectification
- Reduced switching loss
- Easy for MOSFET parallel connection
- Low total harmonic distortion and low stress on each device
- Reduced harmonic filter size
- Modular construction, allows relatively low voltage rating devices

Loss Comparison: MMC **vs** conventional 2-level converter



Power loss comparison of 2-level IGBT converter and MOSFET MMC at 10 kHz, η: % efficiency; NL: normal operation; NL_p2: parallel operation (2 MOSFETs connected in parallel with each other). Input DC voltage is 600V based on the existing cable rating. The total power is 10kW based on the power demand per household. Electrolytic capacitors are used here due to their smaller volume.

3. Simulation and Experimental Results for a 5-level MOSFET MMC

Design of 5-level MMC

Input: V_{DC}=600V, 10kW
Output: V_o=240V_{rms}

Capacitor Sizing

Based on the peak-to-peak energy deviation, the minimal submodule can be derived as:

$$C_{sub} = \frac{1.22 \cdot n \cdot |\bar{S}|}{2\omega \cdot V_{dc}^2 \cdot \Delta V_{max}}$$

C_{sub}=3.3mF, 10% voltage ripple

Arm Inductor Sizing

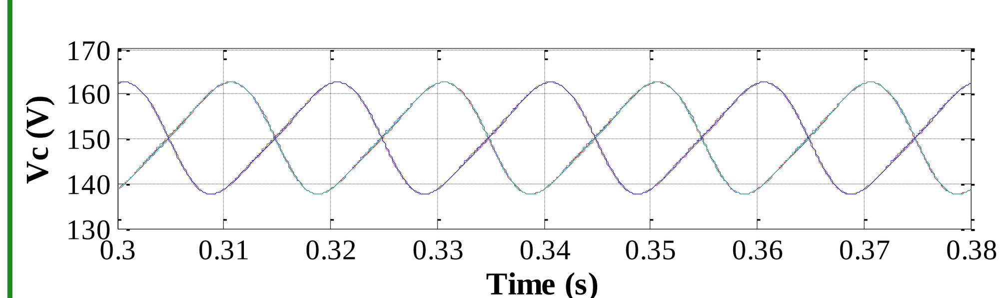
Arm inductor is sized to limit the switching frequency circulating current:

$$L_{arm} = \frac{5n}{2\omega C_{sub} \cdot f_s}$$

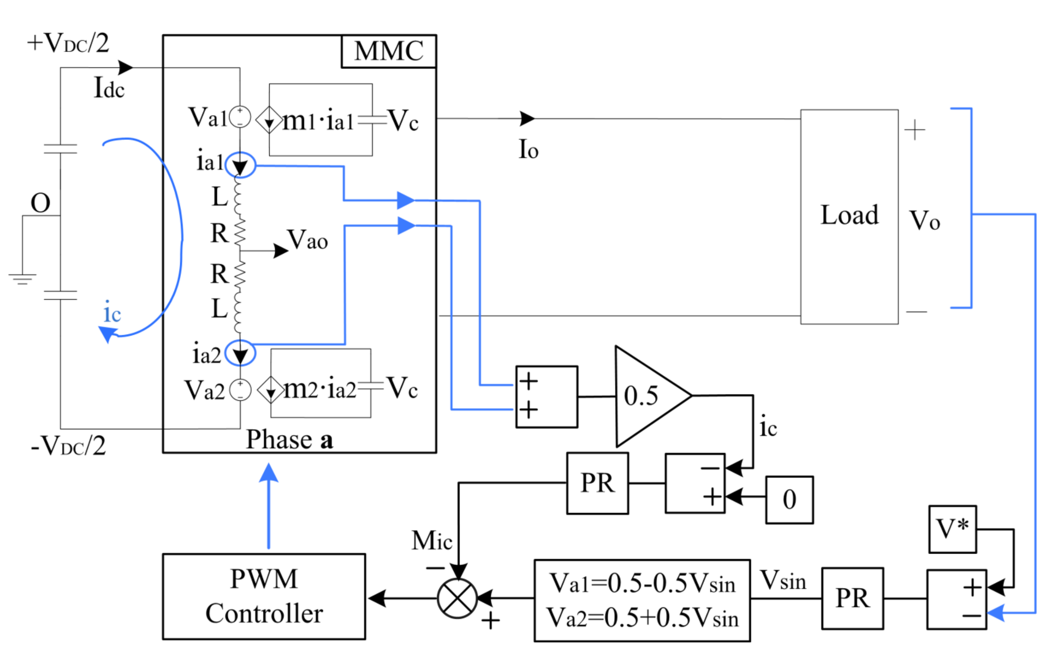
L_{arm}=1.5mH, 5% input current ripple

Submodule Capacitor Balancing

Level-shifted SPWM (POD) with sorting method

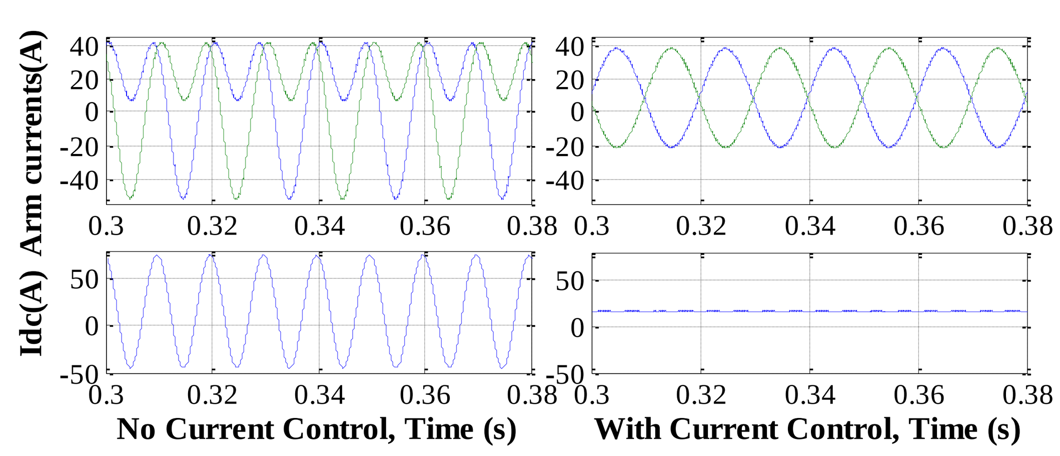


Simulated submodule capacitor voltage balancing for 5-level MMC

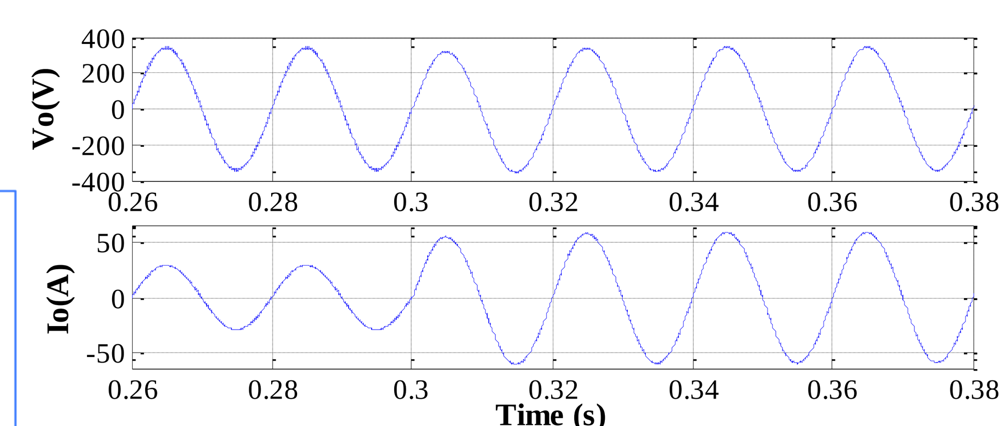


MMC Control Scheme

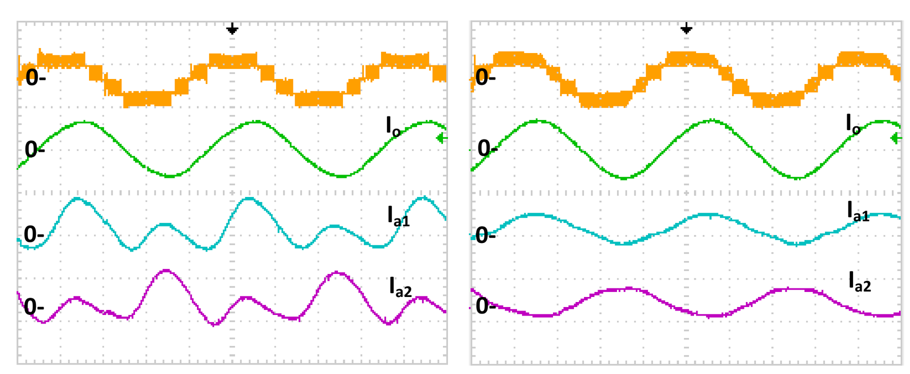
PR controller is used to suppress the 2nd harmonic, which will introduce an infinite gain at a selected resonant frequency.



Circulating Current Suppression Control to eliminate 2nd harmonics

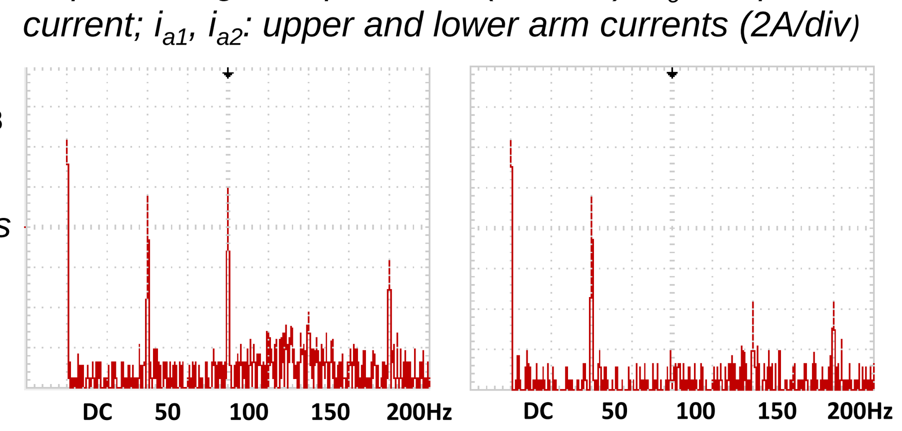


Voltage Regulation, when the power increases from 5kW to 10kW at t=0.3s, voltage stays the same



(a) No Current Control (b) With Current control

5ms/div, Steady-state operation of 5-level MMC, V_a: output voltage of phase A (50V/div); I_o: output load current; i_{a1}, i_{a2}: upper and lower arm currents (2A/div)



FFT analysis of arm currents, 10dB/div. The experimental results show that the second harmonics are eliminated

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