

High-efficiency MOSFET-based MMC for LVDC Distribution Systems

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Abstract—Low-voltage DC (LVDC) systems offer a promising means for improving distribution system efficiency and reliability. The DC-AC conversion stage, however, is one of the main challenges for LVDC networks. A low-voltage modular multilevel converter (MMC) for LVDC distribution systems is proposed in this paper. Analysis is presented to show that its efficiency can exceed that of a conventional 2-level converter. The low voltage rating of each MMC submodule enables MOSFETs to be used in place of IGBTs to reduce power losses. The application of synchronous rectification (SR) further reduces conduction losses. It is shown that device switching frequency reduces as the number of MMC levels is increased. MMC power losses, for different numbers of levels, are compared with those of a conventional 2-level converter. Simulation and experimental results are presented to confirm the mathematical analysis.

Keywords—MMC; LVDC; loss calculation; synchronous rectification; thermal analysis

I. INTRODUCTION

Low-voltage power distribution networks face challenges from increased loads combined with deployment of new technologies. In particular, numbers of high-capacity power electronic interfaces, such as electric vehicle chargers and embedded PV generation, have increased significantly. Compared with conventional low-voltage AC systems, LVDC systems offer several potential benefits, including improved utilisation of cable voltage ratings, and elimination of reactive current and skin effect losses[1-3]. DC distribution also complements the growth of power electronic loads having an implicit DC stage as part of their grid interface [4]. Using DC can eliminate the stand-by losses caused by input transformers inside the adaptors of electronic loads, which are estimated to be approximately 52 TWh/year in the EU-27 countries [5]. Also, the use of higher distribution voltages, and point-of-use regulation in LVDC networks reduces the impact of thermal limits and increases transmission power capacity [1].

Although many new loads are directly suited to DC connection, DC networks will continue to supply a significant portion of conventional AC loads. A major challenge for LVDC systems are therefore the provision of low-loss, high power quality point-of-use DC-AC converters. High conversion efficiencies are required if the conversion losses are not to compromise the benefits of DC distribution. This paper explores the potential of low-voltage multi-level converters to provide high-efficiency, low-distortion DC-AC conversion.

Fig. 1 shows an H-bridge MMC where each phase has 2 arms, each consisting of n submodules (SM) and one arm inductor which is used to suppress the circulating current in the phase[6, 7]. The MMC topology enables it to achieve AC distribution voltage levels using fast, low-voltage, low-resistance MOSFETs in place of the IGBTs used in conventional two-level inverters. Each submodule contains two MOSFETs and one capacitor which acts as an energy storage component that may be inserted in the series path or bypassed according to the switching state of the MOSFETs [8]. The use of multilevel modulation allows the generation of a low-distortion output voltage without the need for output harmonic filters or a high switching frequency [9]. With increased cell number, switching loss is virtually eliminated resulting in a converter design in which conduction loss dominates. Appropriate choice of cell voltage allows the use of low-resistance MOSFETs thereby ensuring converter conduction loss is similar to or less than that which can be achieved with a single high-voltage device. Conduction loss can be further reduced by the use of parallel-connected MOSFETs, facilitated by low switching frequency which reduces the importance of dynamic current sharing. The inherent energy storage of the MMC also allows control and elimination of the DC side 2nd harmonic current, which would result from the connection of conventional single-phase inverters, without the need for bulky LC filters [10].

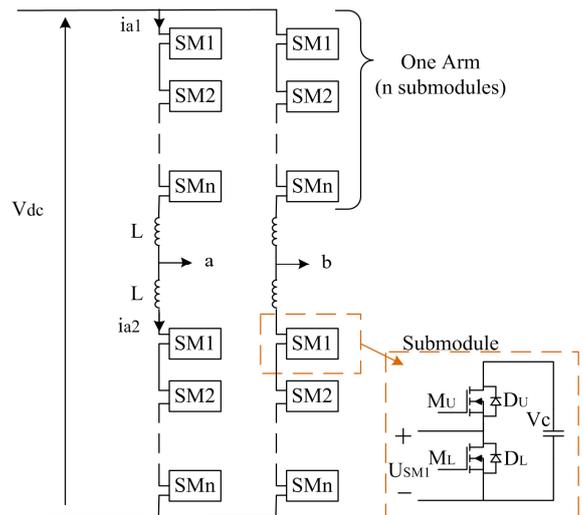


Fig. 1 H-bridge MMC structure

II. LOW-VOLTAGE MMC

The ideal linear model of a single-phase MMC (Fig. 2) assumes that all capacitor voltages are balanced. The upper and lower arm voltages and currents produced by the cascaded submodules are V_{a1} and V_{a2} , and i_{a1} and i_{a2} respectively. Output voltage V_{ao} and current i_a are assumed to be sinusoidal with lagging phase angle φ , and can be expressed as

$$V_{ao} = M \cdot \sin \omega t \cdot \frac{V_{dc}}{2} \quad (1)$$

$$i_a = I_a \sin(\omega t - \varphi) \quad (2)$$

where M is the modulation index.

The arm currents can be expressed as (3) and (4)[11, 12], where i_c is the circulating current in phase 'a'.

$$i_{a1} = i_c + \frac{i_a}{2} \quad (3)$$

$$i_{a2} = i_c - \frac{i_a}{2} \quad (4)$$

With sinusoidal pulse wave modulation (SPWM), the instantaneous arm voltages can be expressed as (5) and (6).

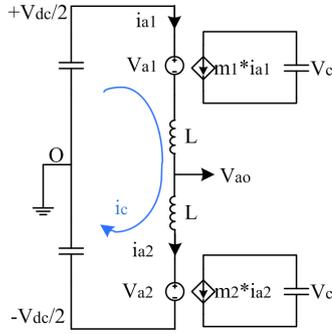


Fig. 2 Ideal linear model of an MMC

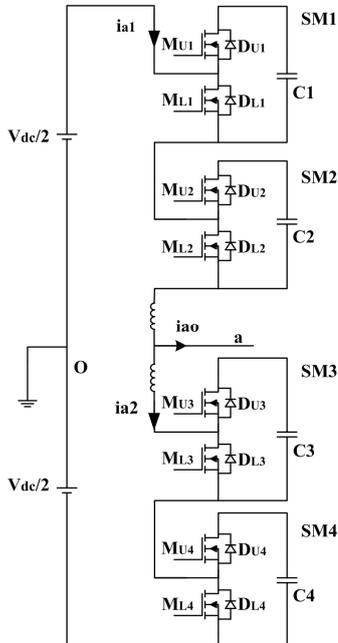


Fig. 3 One phase of a 3-level MMC

Table 1 Submodule Status

V_{a1}	Submodule Status	Gate Signal for $S_{U1/2}$
0	Both are bypassed	Both are '0'
$V_{dc}/2$	One is inserted and one is bypassed	One is '0' and one is '1'
V_{dc}	Both are inserted	Both are '1'

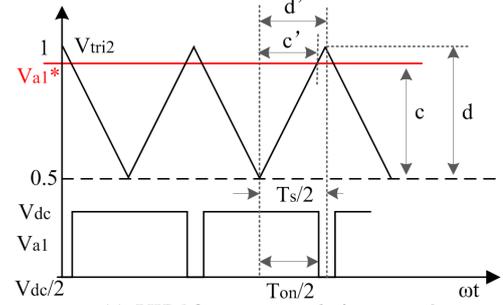
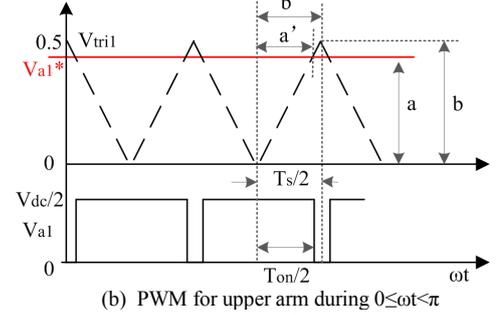
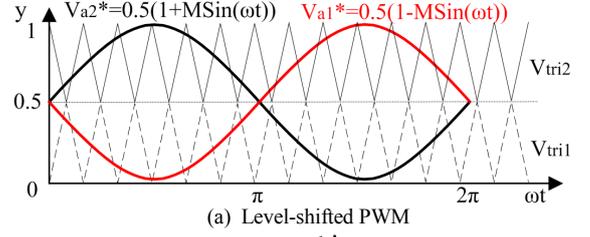


Fig. 4 Level-shifted PWM for 3-level MMC

$$V_{a1} = m_1 \cdot V_C = \left(\frac{1}{2} - \frac{1}{2} M \cdot \sin \omega t \right) \cdot V_C \quad (5)$$

$$V_{a2} = m_2 \cdot V_C = \left(\frac{1}{2} + \frac{1}{2} M \cdot \sin \omega t \right) \cdot V_C \quad (6)$$

To obtain the duty cycles for upper arm switches M_U and M_L , a three-level MMC is illustrated (Fig. 3). Level-shifted SPWM (Fig. 4) is applied to control the switches. There are 2 submodules in one arm, hence the arm voltage can have 3 output levels: 0, $V_{dc}/2$ or V_{dc} , as shown in Table 1.

During the interval $0 \leq \omega t < \pi$, the upper arm voltage V_{a1} has two states: 0 and $V_{dc}/2$. According to Fig. 4(b), the duty ratio d_1 relating to state $V_{dc}/2$ can be deduced as (7)

$$\begin{aligned} d_1 &= \frac{T_{on}/2}{T_s/2} = \frac{a'}{b'} = \frac{a}{b} = \frac{V_{a1}^*}{V_{tri1}} \\ &= \frac{0.5 - 0.5M \cdot \sin \omega t}{0.5} = 1 - M \cdot \sin \omega t \end{aligned} \quad (7)$$

where T_s is the switching period.

According to Table 1, only one submodule is inserted when $V_{a1} = V_{dc}/2$. The probability that SM1 is chosen is $1/C_1^2$, where C_x^m is the number of possible combinations of x items chosen from a set of m items at a time without repetition. Therefore, during $0 \leq \omega t < \pi$, the duty cycle of switch $S_{U1/2}$ is

$$d_{SU} = \frac{1}{C_1^2} \cdot d_1 = \frac{1}{2}(1 - M \cdot \sin \omega t), \quad 0 \leq \omega t < \pi \quad (8)$$

Similarly, during the interval $\pi \leq \omega t < 2\pi$, the upper arm voltage V_{a2} has two states: V_{dc} and $V_{dc}/2$. The duty ratios d_2 and d_3 relating to states V_{dc} and $V_{dc}/2$ are given by (9) and (10) respectively.

$$d_2 = \frac{T_{on}/2}{T_s/2} = \frac{c'}{d'} = \frac{c}{d} = \frac{V_{a2}^* - 0.5}{V_{tri2}} \\ = \frac{0.5 - 0.5 \cdot M \cdot \sin \omega t - 0.5}{0.5} = -M \cdot \sin \omega t \quad (9)$$

$$d_3 = 1 - d_2 = 1 + M \cdot \sin \omega t \quad (10)$$

From Fig. 4(c), duty cycle of $S_{U1/2}$ during $\pi \leq \omega t < 2\pi$ is

$$d_{SU} = \frac{1}{C_1^2} \cdot d_3 + d_2 = \frac{1}{2}(1 - M \cdot \sin \omega t), \quad \pi \leq \omega t < 2\pi \quad (11)$$

In summary, the duty cycles for switch $S_{U1/2}$ and $S_{L1/2}$ are

$$d_{SU} = \frac{1}{2}(1 - M \cdot \sin \omega t) \quad (12)$$

$$d_{SL} = \frac{1}{2}(1 + M \cdot \sin \omega t) \quad (13)$$

For MMC with more than 3-levels, similar method can be used to calculate the duty cycles and the results are the same as (12) and (13).

Submodule switching frequency reduces as the number of levels increases. For a 3-level MMC, the ‘capacitor voltage sorting’ balancing method is used. During intersection of the modulation (V_{a1}) and carrier waveforms, shown in Fig. 4, when arm current is positive, only the submodule with the smallest capacitor voltage V_C would be inserted, or that with the largest V_C would be bypassed [13], so that in one arm only one switch will act at the intersection point and the switching

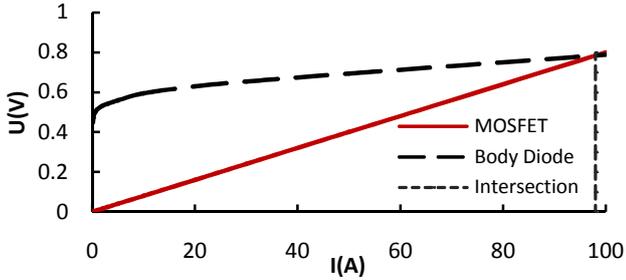


Fig. 5 MOSFET and body diode voltage drop during third quadrant operation

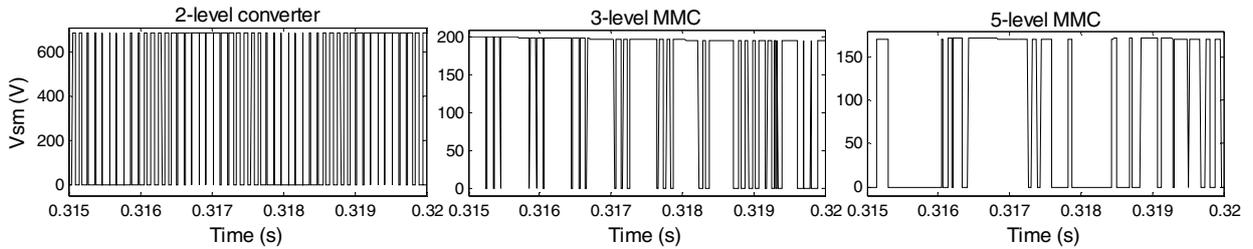


Fig. 6 Simulated submodule voltage (V_{SM1} in Fig. 1) waveforms for 2, 3 and 5-level converters

frequency of each switch is half the carrier frequency. Fig. 6 demonstrates the reduction in device switching frequency achieved with increasing numbers of levels.

III. EFFICIENCY COMPARISON (LOSS CALCULATION)

Self-commutated power devices, such as MOSFETs and IGBTs, have two main power loss components: conduction loss and switching loss. Diodes can be considered as ideal switches at turn-on, so that losses are dominated by conduction and recovery losses.

A. Conduction Loss

Conduction loss is the product of on-state saturation voltage and on-state current. On-state resistance R_{on} can be obtained from manufacturers’ datasheets. IGBT, MOSFET and diode conduction losses can therefore be expressed as

$$P_{con_IGBT} = \frac{1}{T} \int_0^T V_{on}(t) \cdot i_c(t) dt \\ = \frac{1}{T} \int_0^T (V_{ce0} + i_c(t) \cdot R_{on}) \cdot i_c(t) dt \\ = \bar{I}_{av} \cdot V_{ce0} + I_{rms}^2 \cdot R_{on} \quad (14)$$

$$P_{con_MOSFET} = \frac{1}{T} \int_0^T (i_c(t) \cdot R_{on}) \cdot i_c(t) dt \\ = I_{rms}^2 \cdot R_{on} \quad (15)$$

$$P_{con_Diode} = \frac{1}{T} \int_0^T (V_{F0} + i_c(t) \cdot R_{on}) \cdot i_c(t) dt \\ = \bar{I}_{av} \cdot V_{F0} + I_{rms}^2 \cdot R_{on} \quad (16)$$

where V_{ce0} and V_{F0} are the no-load IGBT and diode forward voltage drops respectively, and \bar{I}_{av} and I_{rms}^2 are the average and rms values of load current i_c .

Synchronous Rectification

While operating the MOSFET in the third quadrant, the output characteristics are symmetric to those of first quadrant operation, and the same on-state resistance can be assumed [14]. The reverse conduction characteristic of the MOSFET can be exploited to mitigate conduction losses in the anti-parallel diode which would otherwise compromise the efficiency of a multi-cell MMC. As illustrated in Fig. 5, for instance, the MOSFET (type IRF4668) on-state voltage is lower than across its body diode when the current is approximately 100A [15]. With synchronous rectification, the MOSFET is gated ‘on’ during diode conduction allowing preferential conduction through the low on-state resistance, low-loss MOSFET. Therefore, as shown in Fig. 7 (a) and (b), with switch states $S_U=1, S_L=0$ and $S_U=0, S_L=1$ respectively, current flows through the MOSFET instead of the anti-parallel diodes, which only conduct during dead-time, i.e. $S_U=0, S_L=0$.

B. Switching Loss

Assuming a linear relationship between IGBT turn-on/off energy losses (E_{on}/E_{off}) and the collector current, curve fitting can be used to obtain an energy loss equation based upon device datasheet information. Thus, the IGBT switching losses can be calculated from the product of turn-on/off energy loss E_{on}/E_{off} and switching frequency f_s , as shown in (17).

$$P_{SW_IGBT} = \bar{E}_{switch} \cdot f_s$$

$$= [(K_{on_0} + K_{off_0}) + (K_{on} + K_{off}) \cdot \bar{I}_{av}] \cdot f_s \quad (17)$$

where K_{on_0} and K_{off_0} are the offsets, K_{on} and K_{off} are the gradients used in the curve fitting of the E_{on} and E_{off} respectively.

MOSFET switching losses can be expressed as [16]

$$P_{SW_MOSFET} = \frac{1}{2} I_D V_D (t_{off} + t_{on}) f \quad (18)$$

where t_{on} and t_{off} respectively are the turn-on and turn-off times, which can be obtained from (19) and (20)

$$t_{on} = t_{off} = \frac{Q_{sw}}{I_{GS}} \quad (19)$$

$$Q_{sw} = (Q_{gs} - Q_{g(th)}) + Q_{gd} \quad (20)$$

where Q_{sw} is the switching gate charge increment required as gate voltage increases from its threshold value to the end of its plateau level [17], and I_{GS} is the average gate current.

The Miller plateau gate current is used to approximate the average gate current I_{GS}

$$I_{GS} = \frac{V_{GS} - V_P}{R_g} \quad (21)$$

where V_P is the gate plateau voltage, and R_g is the total gate resistance. Diode reverse recovery loss is given by (22), where Q_{rr} is the reverse recovery charge.

$$P_{rr_D} = Q_{rr} \cdot V_D \cdot f_s \quad (22)$$

C. MMC Power Loss Calculation

Due to synchronous rectification, the diodes only conduct during dead-time. Because dead-time is only 2% of the switching period, the dead-time loss (diode conduction loss) can be ignored. Hence, MMC power losses are mainly comprised of MOSFET conduction and switching losses, and diode reverse-recovery losses. Fig. 8 shows the MMC current waveforms, whilst the power losses for the devices in one submodule are expressed in (23)-(28).

$$\bar{P}_{cond_MU} = \frac{1}{2\pi} \int_0^{2\pi} d_{SU} \cdot (i_{a1}^2 \cdot R_{on_M}) d(\omega t) \quad (23)$$

$$\bar{P}_{cond_ML} = \frac{1}{2\pi} \int_0^{2\pi} d_{SL} \cdot (i_{a1}^2 \cdot R_{on_M}) d(\omega t) \quad (24)$$

$$\bar{P}_{sw_DU} = \frac{1}{2\pi} \int_{\alpha}^{\beta} \frac{Q_{rr}}{I_{test} \cdot V_{test}} \cdot V_C^2 \cdot i_{a1} \cdot f_s d(\omega t) \quad (25)$$

$$\bar{P}_{sw_DL} = \frac{1}{2\pi} \int_{\beta}^{2\pi+\alpha} \frac{Q_{rr}}{I_{test} \cdot V_{test}} \cdot V_C^2 \cdot i_{a1} \cdot f_s d(\omega t) \quad (26)$$

$$\bar{P}_{sw_MU} = \frac{1}{2\pi} \int_0^{2\pi} V_C^2 \cdot i_{a1}^2 \cdot \left(\frac{Q_{sw}/I_{GS}}{I_{test} \cdot V_{test}} \right) \cdot f_s d(\omega t) \quad (27)$$

$$\bar{P}_{sw_ML} = \bar{P}_{sw_MU} \quad (28)$$

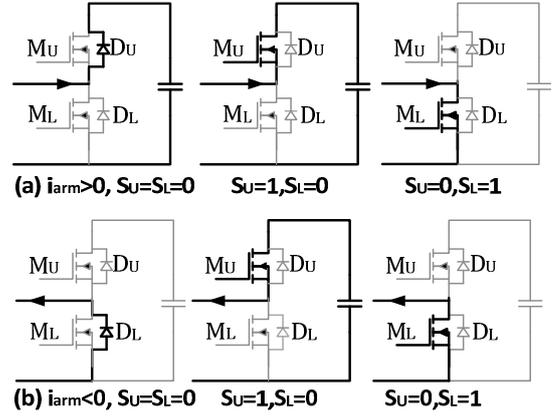


Fig. 7 Submodule current paths in a MOSFET-based MMC (S_U =upper switch, S_L =lower switch and 0/1=off/on)

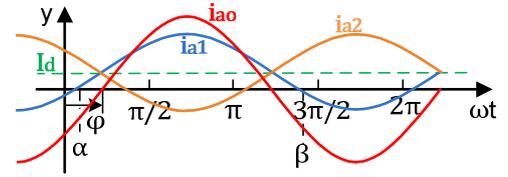


Fig. 8 MMC current waveforms

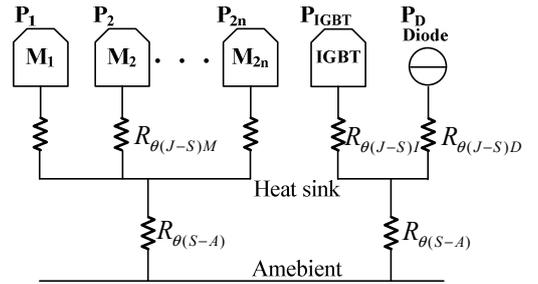


Fig. 9 Thermal equivalent circuit

D. Thermal Calculation

Power losses in the semiconductors result in raised junction temperature. Thermal calculation is used to ensure power device junction temperature remains within its safe range.

Fig. 9 shows the thermal equivalent circuit for MOSFETs and IGBTs. $R_{\square(J-S)}$ denotes the thermal resistance between junction and heatsink, and comprises junction-to-case $R_{\square(J-C)}$ and case-to-heatsink $R_{\square(C-S)}$ thermal resistances, as shown in (29).

$$R_{\theta(J-S)} = R_{\theta(J-C)} + R_{\theta(C-S)} \quad (29)$$

The temperature differences between junction and ambient for MOSFET-based MMC and IGBT-based converters are given by (30) and (31) respectively. $R_{\square(S-A)}$ is the heatsink-to-ambient thermal resistance.

$$T_J - T_{amb} = \sum_{i=1}^{2n} P_i \cdot (R_{\theta(J-S)} + R_{\theta(S-A)}) \quad (30)$$

$$T_J - T_{amb} = P_{IGBT} \cdot (R_{\theta(J-S)IGBT} + R_{\theta(S-A)}) + P_D \cdot (R_{\theta(J-S)D} + R_{\theta(S-A)}) \quad (31)$$

E. Comparison of Losses

Fig. 11 (a) shows the efficiency comparison between a conventional 10kHz 2-level converter and MMC systems with the equivalent switching performance. Input voltage is fixed at 600V and load increases from 3kW to 10kW. For MOSFETs, on-state resistance increases with junction temperature due to decreasing carrier mobility, as shown in Table 2 which details the devices used to obtain the results presented in Fig. 11. In this comparison, the junction temperature used for the calculation is 125°C.

The analytical results show that the efficiency of the MMC increases with the number of levels. In this comparison, the efficiency of an MMC with 5 levels or more exceeds that of the IGBT-based two-level converter. Whilst the focus so far has been the losses in semiconductor devices, there would also be losses associated with passive components: notably the output filter used in a 2-level inverter. Those losses are not taken into account in this paper.

Fig. 11 (b) shows the power loss comparison between a MOSFET-based MMC with parallel-connected devices and an IGBT-based two-level MMC at 125°C junction temperature. In each MMC submodule, two MOSFETs are connected in parallel, as shown in Fig.10. As a result of reduced submodule switching frequency and the positive temperature coefficient characteristic of MOSFETs, the current can be shared equally between the parallel-connected MOSFETs. Equal current sharing is therefore assumed during calculations. Experimental result for current sharing will be presented in Section IV. From the calculated results shown in Fig. 11 (b), the efficiencies of MMC with parallel-connected MOSFETs are significantly higher than that of the 2-level IGBT-based converter.

Table 3 shows a comparison of heatsink requirements for the different converter options when delivering 10kW at an equivalent of 10kHz switching frequency. In each case the heatsink thermal resistance $R_{\theta(S-A)}$ is calculated to maintain the 125°C junction temperature used for loss calculation with an ambient temperature T_{amb} of 30°C.

As shown in Table 3, with the correct choice of MOSFET and with the number of converter levels equal to 5 or more, the required heatsink will be smaller than that of the conventional 2-level converter. Irrespective of the number of levels, the power losses in the MMC using parallel-connected MOSFETs (Fig. 10), and therefore heatsink requirements and dimensions, are dramatically reduced. For example, heatsink volume for a 7-level MMC is half that required for a 2-level converter, and heatsink volume required for a 9-level MMC with parallel-connected MOSFETs is 20 times smaller than that required for a 2-level converter, as indicated in Table 4.

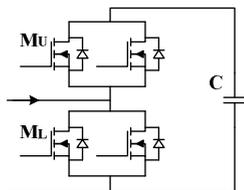
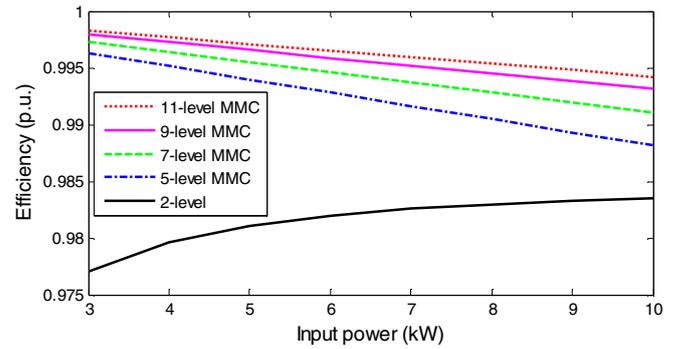
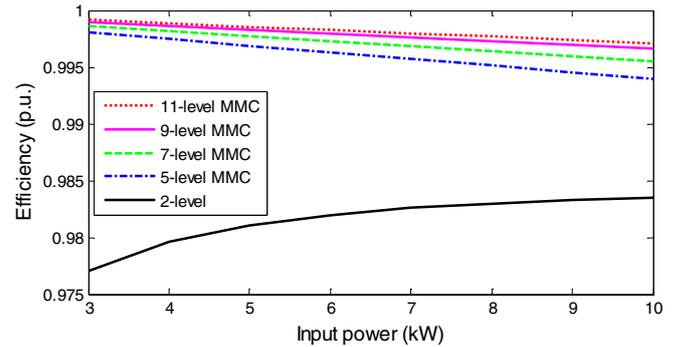


Fig. 10 One MMC submodule with 2 pairs of parallel-connected MOSFETs



(a) MMC with no parallel-connected MOSFETs



(b) MMC with 2 parallel-connected MOSFETs

Fig. 11 2-level IGBT converter and N-level MOSFET MMC efficiencies (Devices: N=2:IRG7PSH50UDPbF; 5:IRFP4768; 7:IRFP4668; 9:IRFP4568; 11:IRFP4110)

Table 2 MOSFET Parameters

Device	IRFP4768	IRFP4668	IRFP4568	IRFP4110
V_{DSS}	250V	200V	150V	100V
$R_{on}^a @25^\circ C$	14.5m Ω	8m Ω	4.8m Ω	3.7m Ω
$R_{on} @80^\circ C$	23.9m Ω	12.8m Ω	7.44m Ω	4.9m Ω
$R_{on} @125^\circ C$	33.9m Ω	17.6m Ω	10.1m Ω	6.9m Ω
$Q_{rr}^b @25^\circ C$	1480nC	633nC	515nC	94nC
$Q_{rr} @125^\circ C$	2260nC	944nC	758nC	140nC

^a R_{on} : MOSFET drain to source on-state resistance

^b Q_{rr} : MOSFET anti-parallel diode reverse recovery charge

Table 3 Required $R_{\theta(S-A)}$ for Different Types of Converters

Converter Type		P_{th} per phase (W)	$R_{\theta(S-A)}$ ($^\circ C/W$)
2-level	IGBT	71.93	0.55
	Diode	16.26	
MMC	5-level	59.41	1.07
	7-level	44.83	1.59
	9-level	34.23	2.25
	11-level	30	2.63
MMC with parallel connected MOSFETs	5-level	30.25	2.61
	7-level	22.42	3.71
	9-level	17.16	5.01
	11-level	14.51	5.91

Table 4 Heatsink Comparison

	Heatsink	Height	Width	Length	$R_{\theta(S-A)}$
2-level	97CN-01000-A-200	40mm	200mm	100mm	0.54°C/W
7-level	43DN-01000-A-200	40mm	100mm	100mm	1.5°C/W
9-level ^a	06DN-00750-A-200	12.5mm	43mm	75mm	4.9°C/W

^a 9-level MMC with parallel-connected MOSFETs

IV. EXPERIMENTAL VERIFICATION

A series of tests were conducted to validate the assumptions used for loss calculations for MOSFET MMC modules. Fig. 12 shows the experimental test rig used to measure the module switching behaviour and losses. It consists of a single MMC module operated as a DC-chopper with an R-L load. The module is mounted on a heatsink for which temperature rise has been pre-calibrated against known dissipation. Module heat sink temperature is used to predict the associated device losses at a range of power levels, thereby avoiding issues associated with direct electrical loss measurements [18]. Experimentally derived power loss predictions can then be compared with those calculated using the method described in Section III.

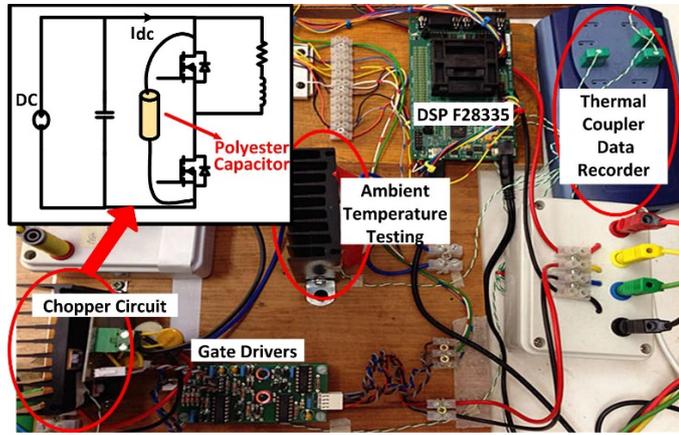


Fig. 12 Experimental test rig for power loss measurement

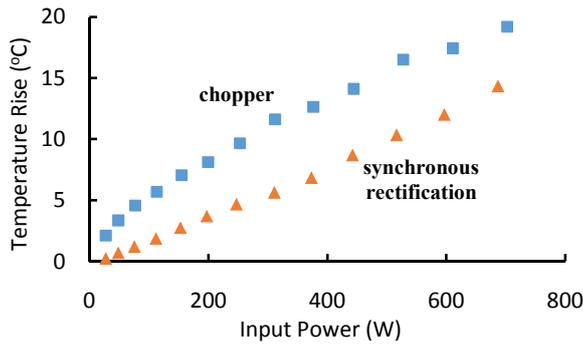


Fig. 13 Thermal performance comparison

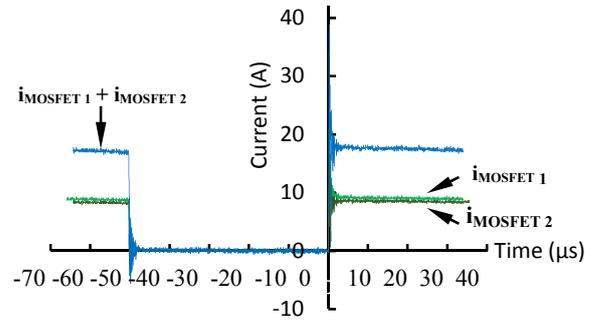


Fig. 14 Current sharing between 2 parallel-connected MOSFETs

A. Synchronous Rectification

Fig. 13 shows module heat dissipation using both normal chopper operation and synchronous rectification, and highlights the reduced loss in the latter case.

B. Current Sharing between Parallel-connected MOSFETs

Because of the MOSFET's positive temperature coefficient, current can be shared equally between parallel-connected MOSFETs. Fig. 14 shows the current sharing of two parallel MOSFETs at 10kHz switching frequency and 50% duty cycle. The drain currents of the two MOSFETs, measured using a Rogowski coil, are practically identical.

Table 5 Chopper Circuit Component Thermal Resistances

MOSFET (IRFB4127PbF)	Junction-to-Case	$R_{\theta(j-c)}=0.4^{\circ}\text{C/W}$
	Case-to-Heatsink	$R_{\theta(c-s)}=0.5^{\circ}\text{C/W}$
Thermal Insulator (Sil-Pad K-10) Thermal Pad @50 psi		$R_{\theta(ins)}=2.01^{\circ}\text{C/W}$
Heat Sink (47DN-01000-A-200)		$R_{\theta(s-a)}=1.7^{\circ}\text{C/W}$

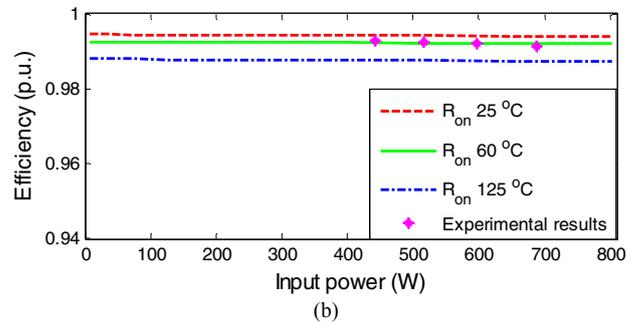
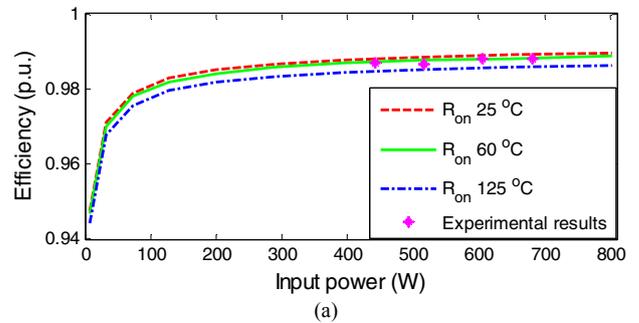


Fig. 15 Comparison of measured and calculated thermal results during (a) normal operation and (b) synchronous rectification

C. Thermal Analysis

In the chopper test rig (Fig. 12), the inductive load is fixed and the input power is increased from 8W to 800W with 50% duty cycle and 10kHz switching frequency. The devices used, and their thermal resistances, are detailed in Table 5.

Based on the loss calculation, the maximum power loss (800W input power without synchronous rectification) is 8.4W, where the on-state resistance of the MOSFET at 25°C junction temperature is adopted. Therefore, the practical junction temperature can be calculated from (32).

$$T_j = T_{amb} + P_{loss} \cdot (R_{\theta J-C} + R_{\theta C-S} + R_{\theta Ins} + R_{\theta HS}) \quad (32)$$

The maximum junction temperature is 63.7°C. Hence, $T_j=60^\circ\text{C}$ is used in the following Section III D.

D. Thermal Measurement Verification

Fig. 15 shows the calculated efficiency based on specific junction temperatures, T_j . The lower temperature limit of $T_j=25^\circ\text{C}$ represents ambient. Whilst a higher value of T_j could be chosen as the upper limit, $T_j=125^\circ\text{C}$ represents a more practical case where temperature rise is not excessive. Calculated efficiency for $T_j=60^\circ\text{C}$ is also shown. This value corresponds to the predicted junction temperature at the thermal dissipation under test. The calculated efficiency curve at $T_j=60^\circ\text{C}$ shows good agreement with the measured data, which also lies within the expected range $25^\circ\text{C} < T_j < 125^\circ\text{C}$.

V. CONCLUSION

It has been demonstrated that with the appropriate choice of devices and number of levels, low-voltage modular multilevel converters (MMC) can achieve very low switching loss without incurring additional conduction loss. These properties have the potential to deliver significant gains in efficiency over conventional two-level DC-AC converters. Experimental tests on one MMC submodule have been used to validate the MMC loss calculations. It has been shown that synchronous rectification results in reduced power loss and that further loss reduction can be achieved by parallel MOSFET connection, which is improved through the use of low switching frequency.

Losses are reduced at the expenses of increased system complexity. Notably the increased number of components and subsystems may impact on manufacturing cost and reliability. However, reliability issues are mitigated by the inherent redundancy which can achieve fault-ride through in multilevel topologies.

The MOSFET-based MMC converter is able to combine the high efficiency and high power quality necessary to overcome the DC-AC stage challenge in LVDC distribution networks.

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