Post - DC Fault Recharging of the H-bridge Modular Multilevel Converter

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Abstract

This paper presents a new recharging strategy for the DC link capacitors of the H-bridge modular multilevel converter (HB-M2C) following DC side faults. The recharging strategy investigated in this paper focuses on the charging algorithm that ensures controlled charging of the DC link capacitors, while ensuring that voltage across the H-bridge cell capacitors remain balanced, and within switching device operating limits. This control strategy limits any potential inrush current from the AC side during re-energizing of the DC link following a DC side fault, without the need of any external circuitry or charging resistors. This may improve the fast recovery of the power networks from DC side faults and minimize the impact on the AC grids. To demonstrate the technical feasibility of the proposed recharging scheme, an H-bridge modular multilevel converter with reverse power blocking capability is simulated.

1 Introduction

Multilevel converters have gained interest from high-voltage DC (HVDC) converter manufacturers and researchers in recent years. They provide a set of features which are suitable for HVDC transmission systems and connection of offshore wind farms, and DC grids [1]. Multilevel converters can synthesize high voltage from small voltage steps and low switching frequency, resulting in low AC side harmonics and high efficiency. As a result it may require a transformer with low insulation and small filter size [2-6].

For more than three levels, diode-clamped converters suffer from voltage imbalance of the DC link capacitors; the problem requires external circuits to maintain voltage balance [7]. This increases system complexity with increasing number of levels [8]-[10]. The effect of stray inductance in the clamping paths is also a problem. The two-switch cell modular multilevel converter has emerged as a viable and acceptable converter for HVDC applications. It has several advantages, such as modular extension to any number of levels and redundancy [11]. However it does not have reverse current block capability, therefore is unable to protect against DC network faults.
HB-M2C has all the advantages of two-switch cell modular multilevel converter plus DC fault reverse blocking capability. This allows the H bridge cell capacitors to remain charged during the fault and does not permit current in-feed from the AC side during DC side faults. This feature permits controlled post-fault recharging of the DC link capacitance from the AC side without the use of AC side contactors and resistors; exploiting the redundant switch state available within the converter to perform controlled charge while maintaining the cell capacitor voltages.

2 Review of the H-bridge modular multilevel converter

The three-level HB-M2C uses two cells per arm, and each cell capacitor and switching devices must not experience voltage stress of more than $\frac{1}{2}V_{dc}$, see Fig. 1. Therefore an n-level version of this converter requires n-1 cells per arm, and each switch and capacitor blocks V_{dc}/n. The HB-M2C can be controlled using the same modulation strategies as the two-switch M2C [1, 12-14].

3 DC link Post-fault recharging method

This section illustrates the proposed charging strategy with respect to the H-bridge modular converter depicted in Fig. 1. C_d represents the main DC link capacitors or total effect of DC cable distributed stray capacitors. I_d and I_{dmax} represent DC side charging current and its maximum value. v_a, v_b and v_c , and i_a, i_b and i_c denote three phase voltages and currents respectively. The proposed charging algorithm is summarised as follows:

- First, the phase voltage with maximum and minimum values must be identified using $V_{max} = \max(v_a, v_b, v_c)$ and $V_{min} = \min(v_a, v_b, v_c)$.
- To prevent excessive current flow in the DC side, the DC side charging current I_d is restricted exploiting converter redundant switch states. When $v_a = V_{max}$, $i_a > 0$ and $I_d < I_{dmax}$, bypass the upper arm cell capacitors of the phase A and block all the lower arm cell capacitors. Since each arm of the H-bridge modular converter supports the full DC link voltage which higher than the peak phase of the AC voltage, there is no risk of excessive inrush current from the AC side. Hence controlled charging of the DC side capacitor is achieved.
- When $V_{min} < v_a < V_{max}$ and $I_d < I_{dmax}$, block all the cell capacitors of the phase A as the DC side capacitors will be charged from another phase with maximum phase voltage as previous explained with respect to phase A.
- When $v_a = V_{min}$ and $I_d < I_{dmax}$, the upper arm cell must be inhibited and lower arm cells must be switched on to charge the DC side capacitors.

- When the DC side charging current exceeds I_{dmax} (I_d>I_{dmax}) all the cells of the three phases must block.

The same algorithm is applied to phases B and C. Tables 1 and 2 summarise the proposed charging algorithm during re-energization of the DC side and capacitor voltage balancing when the DC link is fully established.

4 Cell capacitor voltage balancing when the DC link voltage is fully established

In the illustrative version of the HB-M2C in Fig. 1 capacitor voltage balancing is normally achieved using four redundant switch states that produce a zero voltage level depicted in table 2 and Fig. 2, taking into account the polarity of the AC output currents.

The current paths through the cells of the upper and lower arms are illustrated in Fig. 2 when the redundant switch states associated with the zero voltage levels are used. It can be observed that these cells are used as the energy tank

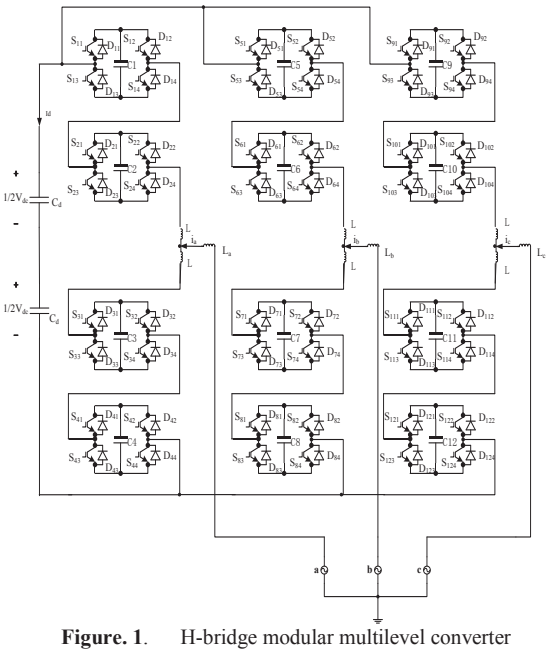


Figure. 1. H-bridge modular multilevel converter

Table 1: Switching states of phase a for DC link capacitance recharging

charging voltage from phase a	S_{11}	S_{12}	S_{21}	S_{22}	S_{31}	S_{32}	S_{41}	S_{42}
u_a	1	1	1	1	0	0	0	0
$-u_a$	0	0	0	0	1	1	1	1
0	0	0	0	0	0	0	0	0

Table 2: Effect of redundant switch states on capacitor voltage

Switch states	Current direction	Current path	Connected capacitors
① 1001110000000000	i_a>0	S_{11}, C_1, S_{14}, S_{21}, D_{22} and C_d	C_1 ↓
② 1100100100000000	i_a>0	S_{11}, D_{12}, S_{21}, C_2, S_{24} and C_d	C_2 ↓
③ 0000000010011100	i_a<0	S_{31}, C_3, S_{34}, S_{41}, D_{42} and C_d	C_3 ↓
④ 0000000011001001	i_a<0	S_{31}, D_{32}, S_{41}, C_4, S_{44} and C_d	C_4 ↓

Note that switch state '1' means when switch S_{ij} is on and '0' means when it is off, where *j=1,4* and *i=1 to n*

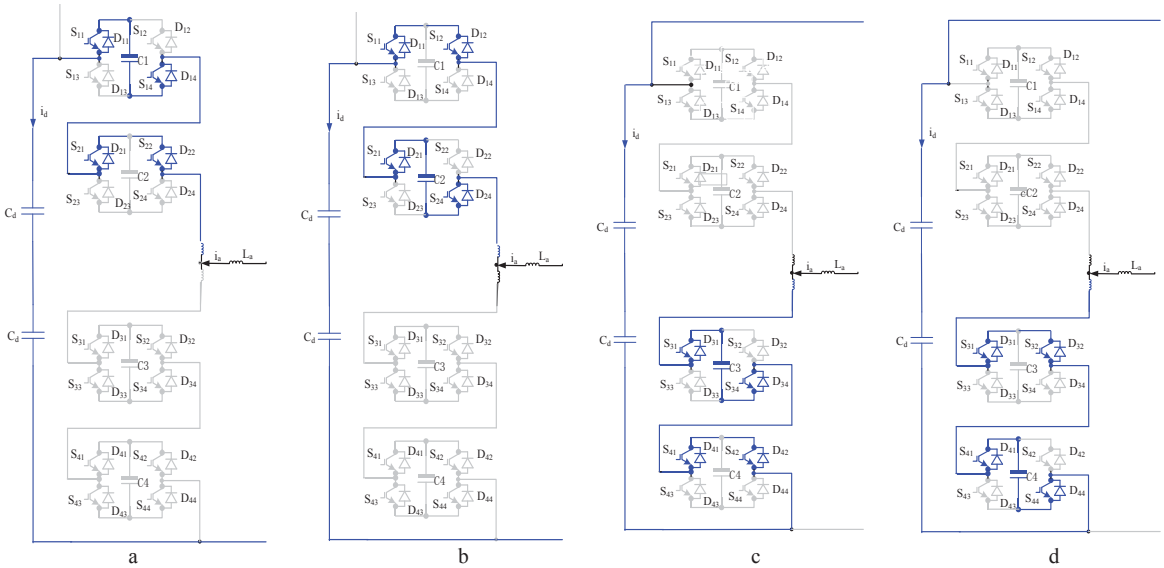


Figure. 2 Current path of phase a at redundant switch state during DC link recharging period

alternatively during the power exchange between the AC and DC sides. Therefore these states can be exploited effectively for balancing purpose as described [1, 15, 16]. In each cell of the HB-M2C (S_{i1} and S_{i3}) and (S_{i2} and S_{i4}) operate as complementary pairs. Turning on S_{i1} precludes S_{i3} from being on simultaneously, where i = 1 to 2n and n is the number of H-bridge cells per arm (therefore 2n cells per phase).

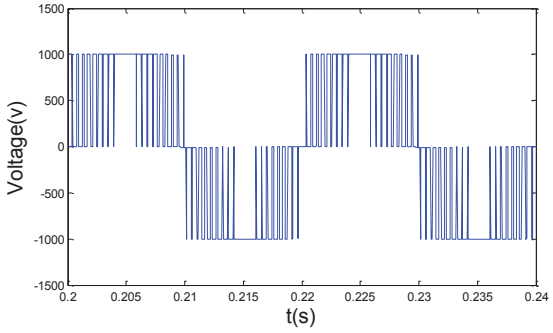
5 Performance Evaluation

This section investigates the technical feasibility of the proposed post fault recharging scheme for the HB-M2C. A three-level HB-M2C with a 2kV DC link voltage, 8mH arm inductor, and 2.2mF cell capacitor is used in this investigation. During normal operation the converter is controlled using multilevel pulse width modulation, with a 2.3kHz switching frequency. Whilst during recharge period the converter is controlled based on peak DC link current control as illustrated section 3.

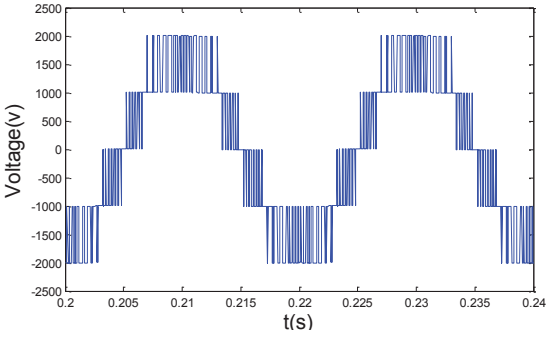
A) Case I: Normal operation

Fig. 3 displays simulation results obtained from the illustrative version of the HB-M2C based on three-levels, operating at 0.9 modulation index and 0.8 power factor lagging. Figs. 3a and 3b show phase and line voltage at the converter terminal. Fig. 3c shows the HB-M2C supplies high quality current waveforms to the load.

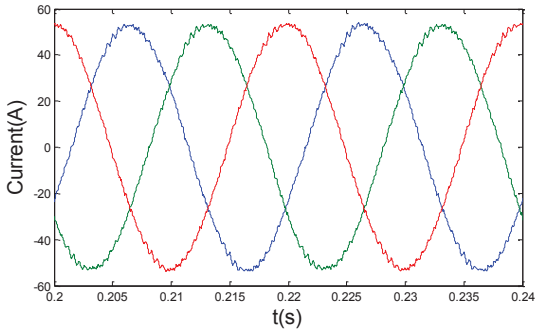
It is observed from Figs. 3a to 3b that there is no switching of more than one voltage level; this ensures minimum dv/dt at the AC side. Fig. 3d shows a sample current waveform in one switch of the H-bridge cells. This shows the switching devices of the three-level HB-M2C operate for half the fundamental cycle. Contrary to the two-switch M2C, this situation is expected to be valid in any HB-M2C regardless of the number of cells. As a consequence, semiconductor losses are expected to be higher. Fig. 3e shows that the voltage stresses across the 12 cell capacitors of the three phases remain balanced and settled around ½Vdc.



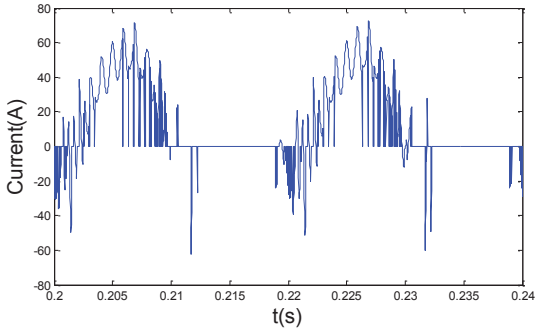
a. Output voltage of phase 'A'



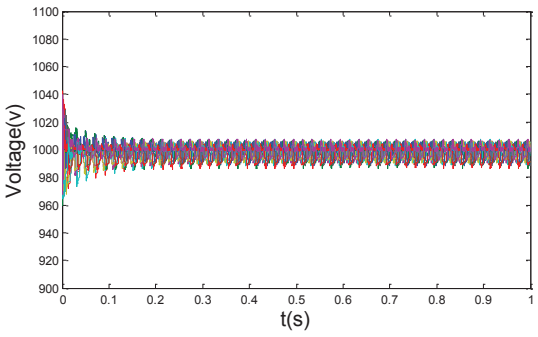
b. Line to line voltage



c. Current waveforms



d. Current waveform of in the switch of the top cell of HB-M2C



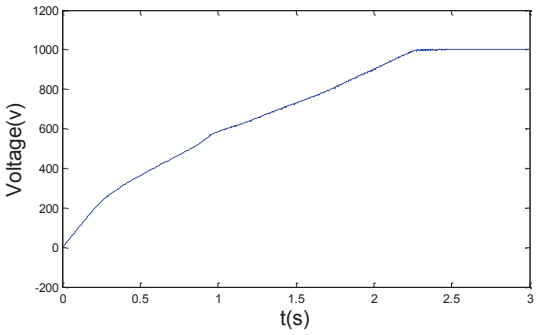
e. voltage across cell capacitors with different initial voltage

Figure. 3 Waveforms illustrate HB-M2C operation during normal operation (0.9 modulation index and 0.8 power factor lagging)

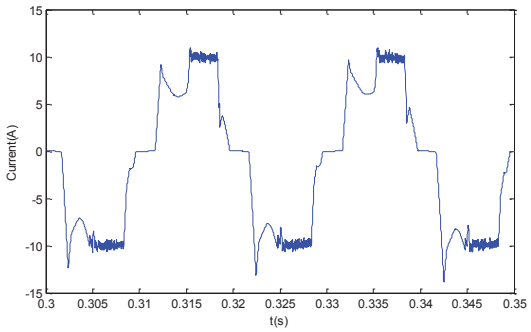
B) Post-fault DC link capacitor recharging

To demonstrate the viability of the presented DC link charging scheme during shutdown and post-fault DC link recharging, this section presents simulation results obtained during charging up of the HB-M2C DC link (Fig. 4). Figs. 4a and 4b present the DC link voltage and AC current during charge up.

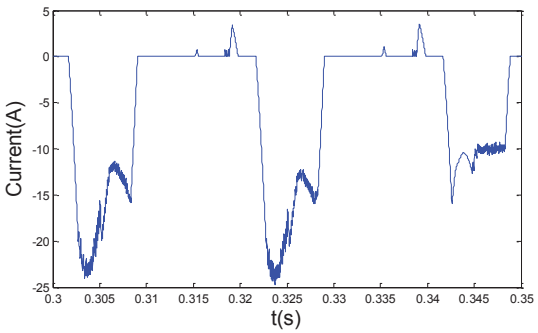
Based on the peak current control strategy, the charging current is limited around the set point (fig.4d-4f) and the voltage across the DC link capacitor increases gradually, at a rate set by the maximum charging current $I_{dmax.}$ Balance between cell capacitors is maintained.



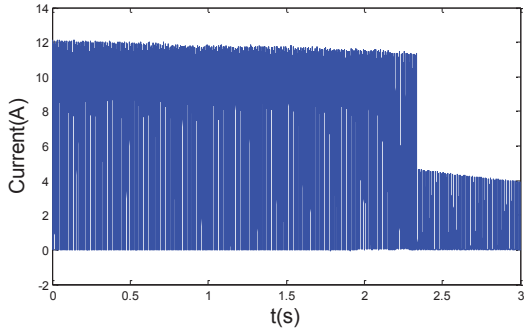
a. Voltage across DC link capacitance



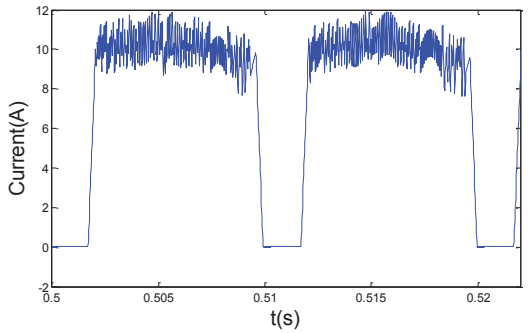
b. Steady charging current



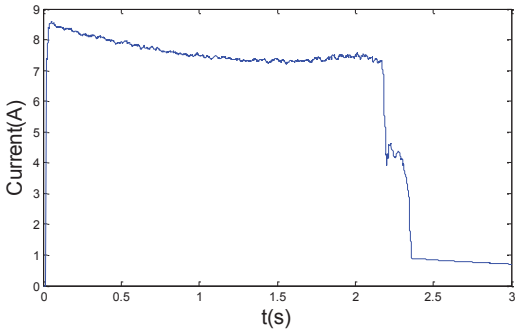
c. lower arm charging current of phase a



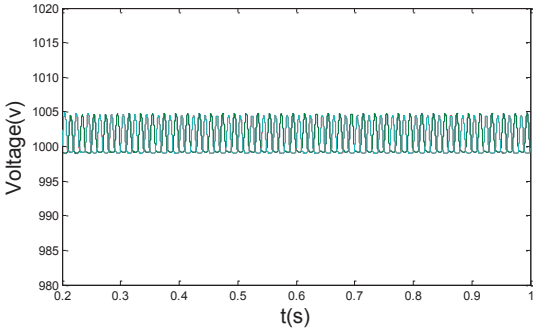
d. DC link recharging current



e. Expanded version of DC link recharging current



f. average current of DC link recharging



g. Voltage across cell capacitors

Figure. 4 Voltage and current waveforms during DC link recharging

6 Conclusions

A new recharging strategy for the DC link capacitors of the H-bridge modular multilevel converter following a DC side fault is presented. It ensures controlled charge of the DC link capacitors while ensuring that voltages across the H-bridge cell capacitors remain balanced. The inrush current from the

AC side is limited, without any external circuitry. The recharging algorithm has been verified by simulation. It improves fast recovery of power networks after a DC fault.

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