An Investigation of High Efficiency DC-AC Converters for LVDC Distribution Networks

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Keywords: LVDC, MMC, Loss Calculation, Capacitor Voltage Balance Control.

Abstract

Low voltage DC (LVDC) distribution systems offer improved efficiency and reliability in smart grids. A major challenge facing LVDC systems is DC-AC conversion. A study of an effective low voltage DC-AC converter is therefore presented. Modular Multilevel Converter (MMC) performance (in particular power loss) is compared with a conventional IGBT-based 2-level converter and its advantages highlighted. A phase-shifted sinusoidal PWM based individual voltage balancing strategy for the MMC is presented. A proportional-resonant controller is introduced to eliminate the 2nd harmonic circulating current in the H-bridge MMC converter.

1 Introduction

Electricity distribution networks must adapt to accommodate increasing loads and the connection of new technologies such as embedded generation, energy storage and electric vehicle (EV) charging. LVDC distribution systems provide a promising solution to improve distribution system efficiency.

DC better utilises conductor voltage rating, thereby increasing power capacities. Additionally, there are no reactive power, frequency stability and skin effect issues in DC networks. Use of power electronics to provide point-of-use regulation of AC supplies can eliminate reactive and harmonic power flows whilst maintaining user power quality. As shown in Figure 1, DC distribution can minimise the conversion stages required to connect devices such photovoltaic (PV) and EV chargers.

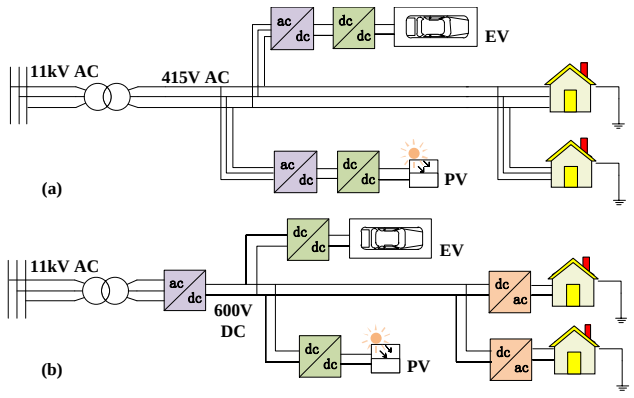

Figure 1: (a) A conventional LVAC distribution system
(b) A proposed LVDC distribution network

The types of loads attached to power systems are changing. Household appliances such as TVs, DVDs, etc., require DC. Appliances, such as machine drives, need variable output frequency, achieved by converting AC to DC and DC to variable frequency AC using power electronics converters [1]. For these kinds of loads, conversion stages can be minimised with DC a distribution network. Resistive loads for heating and lighting can operate using both AC and DC.

A major challenge for LVDC distribution networks is the DC to AC power conversion stage, which must achieve high efficiency whilst meeting user power quality requirements.

2 DC-AC Converters

2.1 Conventional IGBT-based 2-level converter

Figure 2 shows a typical 2-level IGBT-based voltage source converter (VSC). Each phase has two series-connected IGBTs which are operated complementarily. Each IGBT is rated to support the DC link voltage, V_{dc}, and is switched at the carrier frequency.

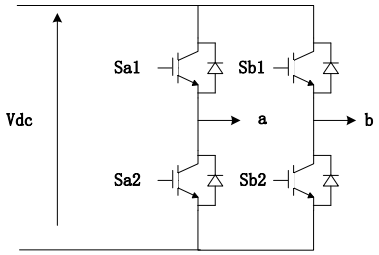

Figure 2: Conventional 2-level converter

Whilst the structure and control method are relatively simple, it has significant disadvantages [2]. Firstly, a bulky passive AC filter is required to suppress undesired harmonics whilst high dv/dt causes EMC disturbance and large voltage and current stresses on each switch. The converter also has high switching loss. Finally, in the event of a DC bus short circuit, the DC capacitor stored energy leads to high DC fault current.

2.2 MOSFET-based modular multilevel converter

The modular multilevel converter (MMC) is an emerging technology for medium- and high-voltage applications [3]. It is suited to LVDC distribution systems since it offers low switching loss, and enables relatively high voltage operation with low harmonic content without the use of AC filters.

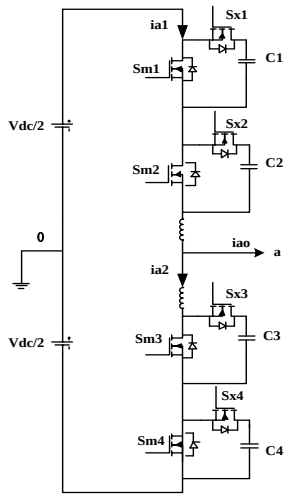

Figure 3: One phase of a three-level MMC

Each cell of the three-level MMC shown in Figure 3 is composed of two switching devices which must operate in a complementary manner. Assuming the DC source midpoint 0 to be the output voltage reference, 6 switch combinations are available to generate the three output voltage levels 0 and $\pm V_{dc}$. At any time, switches are controlled so that the upper and lower arm voltages sum to V_{dc}. Compared with 2-level converters, this topology offers the following features [4]:

- Modular construction: within each module, the voltage level is clamped and may be set to be compatible with each device's voltage rating. The identical modular cells are scalable to different output voltage levels by using a suitable control strategy.
- Low total harmonic distortion and low stress on each cell.
- Smaller AC filters: with increased voltage levels, harmonic filter size can be decreased, leading to a significant cost reduction.

2.3 Loss calculation of two kinds of converters

Estimation of power converter losses is important for thermal circuit sizing and assessment of conversion efficiency [5]. Also, if replacing a conventional 2-level converter with and MMC, there should be no increase in losses. Loss calculations for both converter topologies are therefore presented.

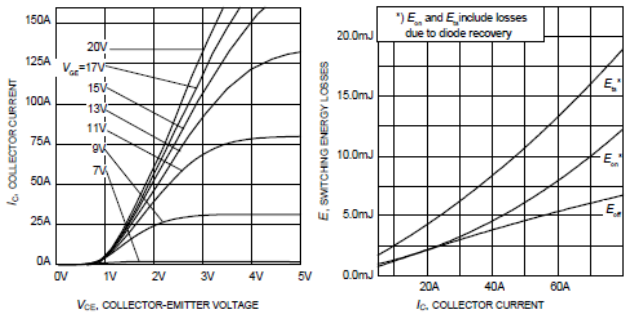

Figure 4:(a) Output characteristic (b) IGBT Switching loss [6]

MOSFETs and IGBTs have two main power loss components: conduction loss and switching loss. Diode losses consist predominately of conduction and recovery losses [2].

A. Conduction Loss

Power dissipation during conduction can be obtained by multiplying the on-state saturation voltage and current.

$$P_{cond} = V_{on} \cdot i_{on} \tag{1}$$

The on-state voltage for an IGBT can be expressed as:

$$V_{on\_IGBT} = V_{ce0} + I_c \cdot R_{on} \tag{2}$$

where device forward resistance R_{on} and IGBT forward voltage drop V_{ce0} are obtained from an output characteristic, such as that shown in Figure 4(a), knowing the collector current I_c. Similarly, MOSFET and diode on-state voltages, V_{on_MOSFET} and V_F respectively, are:

$$V_{on\_MOSFET} = I_c \cdot R_{on} \tag{3}$$

$$V_F = V_{F0} + I_c \cdot R_{on} \tag{4}$$

where V_{F0} is the diode no-load forward voltage drop.

Switching device conduction loss is therefore calculated as:

$$\begin{aligned} P_{con} &= \frac{1}{T}\int_0^T V_{on}(t) \cdot i_c(t)dt \\ &= \frac{1}{T}\int_0^T V_{ce0} \cdot i_c(t)dt + \frac{1}{T}\int_0^T R_{on} \cdot i_c^2(t)dt \\ &= V_{ce0} \cdot \bar{I}_{av} + R_{on} \cdot I_{rms}^2 \end{aligned} \tag{5}$$

where T is the fundamental period and $\bar{I}_{av}$ and I_{rms}^2 are the average and rms values of collector current i_c in the switching device over one fundamental period.

IGBT, MOSFET and diode conduction losses are therefore:

$$P_{con\_IGBT} = \bar{I}_{av} \cdot V_{ce0} + I_{rms}^2 \cdot R_{on} \tag{6}$$

$$P_{con\_MOSFET} = I_{rms}^2 \cdot R_{on} \tag{7}$$

$$P_{con\_Diode} = \bar{I}_{av} \cdot V_{F0} + I_{rms}^2 \cdot R_{on} \tag{8}$$

B. Switching Loss

Switching power loss occurs during a power device's turn-on and turn-off switching transitions. As shown in Figure 4(b) for an IGBT, switching energy loss is given as a function of collector current. Diode recovery losses are already included in total energy loss E_{ts}. Therefore, IGBT switching loss is:

$$E_{switch}(t) = E_{on}(t) + E_{off}(t) + E_{rr}(t) = K_{ts} \cdot i(t) \tag{9}$$

where E_{on}, E_{off} and E_{rr} denote the turn-on, turn-off and diode reverse recovery energy losses, and K_{ts} is the slope of total energy loss E_{ts}. Average IGBT power loss $\bar{P}_{switch}$ can be expressed as:

$$\bar{P}_{switch} = K_{ts} \cdot \bar{I}_{av} \cdot f_s \tag{10}$$

where f_s is the switching frequency.

For a MOSFET, however, switching energy loss curves such as Figure 4(b) are not available. The relationship between drain current and drain-source voltage during turn-on and turn-off can however be presented as in Figure 5 [7], which reveals that during the turn-on transient, the drain current I_D increases to the value demanded by the load and that the gate voltage is clamped. The drain-source voltage V_{DS} then begins to reduce. Turn-on loss is therefore obtained by integrating the product of I_D and V_{DS} during period t_{on}. Similarly, turn-off switching loss may be calculated using I_D and V_{DS} during t_{off}.

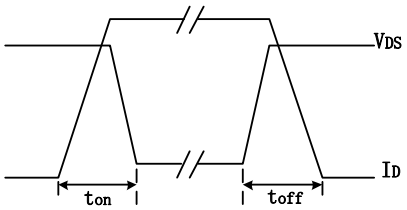

Figure 5: Typical switching waveforms of a MOSFET

Assuming the increase and decrease of voltage and current are linear during the turn-on and turn-off periods, as shown in Figure 5, the following equations can be deduced.

$$E_{on}(t) = \frac{1}{2}V_{DC} \cdot i(t) \cdot t_{on} = \frac{1}{2}{V_{DS}}^2 \cdot i(t)^2 \cdot (\frac{t_{on_N}}{I_{test} \cdot V_{test}}) \quad (11)$$

Average switching energy and power losses are:

$$\bar{E}_{switch} = \frac{1}{2}{V_{DS}}^2 \cdot \bar{I}^2 \cdot (\frac{t_{on_N}+t_{off_N}}{I_{test} \cdot V_{test}}) \quad (12)$$

$$\bar{P}_{switch} = \frac{1}{2}{V_{DS}}^2 \cdot \bar{I}^2 \cdot (\frac{t_{on_N}+t_{off_N}}{I_{test} \cdot V_{test}}) \cdot f_s \quad (13)$$

where t_{onN} and t_{offN} indicate the turn-on and turn-off times under test voltage V_{test} and test current I_{test} conditions.

For the MOSFET freewheeling diode, average reverse recovery power $\bar{P}_{RR}$ is calculated using reverse recovery charge Q_{RR} [7].

$$\bar{P}_{RR} = Q_{RR} \cdot V_{DS} \cdot f_s \quad (14)$$

2.3.1 Loss calculation for an IGBT 2-level converter

The sinusoidal PWM control method is used for the conventional 2-level converter shown in Figure 2. A triangular carrier wave with peak amplitudes of ±1 is assumed and the modulation function v_{sin} and load current i_a are:

$$v_{sin} = M \cdot \sin \omega t \quad (15)$$

$$i_a = I_o \sin(\omega t - \varphi) \quad (16)$$

The duty cycles d_{a1} and d_{a2} of switches S_{a1} and S_{a2} are:

$$d_{a1} = \frac{1}{2} + \frac{1}{2}M \cdot \sin \omega t \quad (17)$$

$$d_{a2} = \frac{1}{2} - \frac{1}{2}M \cdot \sin \omega t \quad (18)$$

During carrier period T_s switch S_{a1} conducts for time $d_{a1}T_s$ whilst switch S_{a2} conducts for time $(1\text{-}d_{a1})T_s$. When i_a>0 ($\varphi \rightarrow \pi+\varphi$), S_{a1} and D_{a2} conduct. When i_a<0 ($\pi+\varphi \rightarrow 2\pi+\varphi$), D_{a1} and S_{a2} conduct.

Based on (6), the average conduction losses for the IGBT and diode can be estimated as:

$$\bar{P}_{cond\_Sa1} = \frac{1}{2\pi}\int_{\varphi}^{\varphi+\pi} d_{a1} \cdot (i_a^2 \cdot R_{on} + V_{ce0} \cdot i_a) d(\omega t) \quad (19)$$

$$\bar{P}_{cond\_Da1} = \frac{1}{2\pi}\int_{\varphi+\pi}^{\varphi+2\pi} d_{a1} \cdot (i_a^2 \cdot R_{on} + V_{f0} \cdot i_a) d(\omega t) \quad (20)$$

$$\bar{P}_{cond\_Sa2} = \frac{1}{2\pi}\int_{\varphi+\pi}^{\varphi+2\pi} d_{a2} \cdot (i_a^2 \cdot R_{on} + V_{ce0} \cdot i_a) d(\omega t) \quad (21)$$

$$\bar{P}_{cond\_Da2} = \frac{1}{2\pi}\int_{\varphi}^{\varphi+\pi} d_{a2} \cdot \left(i_a^2 \cdot R_{on} + V_{f0} \cdot i_a\right) d(\omega t) \quad (22)$$

According to (9) and (10), the total switching loss:

$$\bar{P}_{ts} = \bar{E}_{ts} \cdot f_s = f_s \cdot \frac{1}{2\pi}\int_0^{2\pi} K_{ts} \cdot i_a(t) d(\omega t) \quad (23)$$

The total loss for one IGBT with freewheeling diode is:

$$\bar{P}_{IGBT} = \bar{P}_{cond\_Sa1} + \bar{P}_{cond\_Da1} + \bar{P}_{ts} \quad (24)$$

2.3.2 Loss calculation for a MOSFET M2C

An MMC requires the PWM control to generate multi-level voltage output. Well-known multi-carrier PWM methods are Phase Shifted (PhS), Phase Disposition (PD), Phase Opposition Disposition (POD), and Alternative Phase Opposite Disposition (APOD). For an n-level MMC, n-1 triangular carriers with the same frequency and amplitude are arranged to produce n-level voltage output.

In PhS PWM, all carriers are phase shifted from each other by 360°/(n-1), as shown in Figure 6(a). PhS-PWM leads to lower output voltage distortion for all modulation indices [8].

In PD-PWM , all carriers have the same phase, as shown in Figure 6(b). PD-PWM achieves the lowest line harmonic voltage distortion amongst the disposition methods [9].

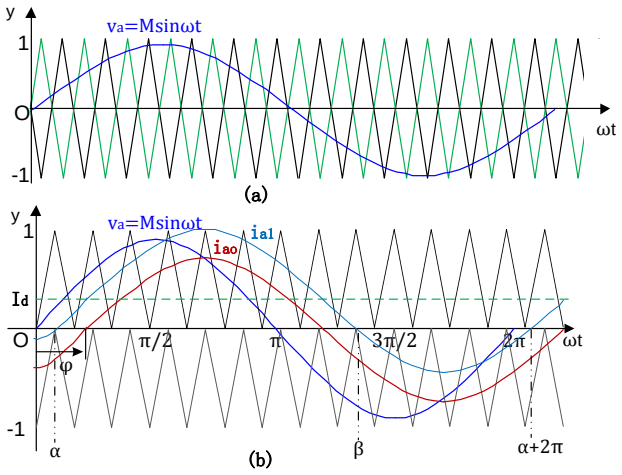

Figure 6: Three-level MMC carrier waveforms
(a) PhS-PWM (b) PD-PWM

In Figure 3, the duty cycles d_{m1} and d_{x2} for cell switches S_{m1} and S_{x1} are:

$$d_{m1} = \frac{1}{2}(1 + M \cdot \sin \omega t) \quad (25)$$

$$d_{x1} = 1 - d_{m1} = \frac{1}{2}(1 - M \cdot \sin \omega t) \quad (26)$$

Upper and lower arm currents, i_{a1} and i_{a2}, are defined as:

$$i_{a1} = I_d + \frac{I_a}{2}\sin(\omega t + \varphi) \quad (27)$$

$$i_{a2} = I_d - \frac{I_a}{2}\sin(\omega t + \varphi) \quad (28)$$

The arm currents consist of a DC component I_d and a component at the fundamental frequency which is determined by AC-side output current I_a [10]. These arm currents determine whether the MOSFET or the diode conducts. When i_{a1}>0, S_{m1} or D_{x1} conducts. When i_{a1}≤0, D_{m1} or S_{x1} conducts. As shown in Figure 6(b), phase angle φ exists between i_{ao} and V_a. Thus, for arm current i_{a1}, α and β can be obtained be setting i_{a1}=0. The following can be deduced:

ωt: α → β, i_{a1}>0	S_{m1} or D_{x1} conducts
ωt: β → α +2π, i_{a1}≤0	D_{m1} or S_{x1} conducts

The average conduction loss during one modulation period:

$$\bar{P}_{cond\_Sm1} = \frac{1}{2\pi}\int_{\alpha}^{\beta} d_{m1} \cdot (i_{a1}^2 \cdot R_{on\_M}) d(\omega t) \quad (29)$$

$$\bar{P}_{cond\_Dm1} = \frac{1}{2\pi}\int_{\beta}^{2\pi+\alpha} d_{m1} \cdot (i_{a1}^2 \cdot R_{on} + V_{f0} \cdot i_{a1}) d(\omega t) \quad (30)$$

$$\bar{P}_{cond\_Sx1} = \frac{1}{2\pi}\int_{\beta}^{2\pi+\alpha} d_{x1} \cdot (i_{a1}^2 \cdot R_{on\_M}) d(\omega t) \quad (31)$$

$$\bar{P}_{cond\_Dm1} = \frac{1}{2\pi}\int_{\alpha}^{\beta} d_{x1} \cdot (i_{a1}^2 \cdot R_{on} + V_{f0} \cdot i_{a1}) d(\omega t) \quad (32)$$

Switching losses are calculated based on (11)-(14):

$$\bar{P}_{switch} = \frac{1}{2} {V_C}^2 \cdot {\bar{\imath}_{a1}}^2 \cdot \left(\frac{t_{on_N} + t_{off_N}}{I_{test} \cdot V_{test}}\right) \cdot f_s + Q_{RR} \cdot V_C \cdot f_s \quad (33)$$

The total power loss for one cell is therefore:

$$\bar{P}_{MOSFET} = \bar{P}_{cond\_Sm1} + \bar{P}_{cond\_Dm1} + \bar{P}_{cond\_Sx1} + \bar{P}_{cond\_Dm1} + \bar{P}_{switch} \quad (34)$$

2.3.3 Loss calculation results

Table 1 compares the calculated losses for the conventional IGBT 2-level converter and the MOSFET-based MMC. In both cases V_{dc}=600V , I_{a_rms}=50A, f_s=10kHz, M=1 and φ=0°.

Converter	No. of Levels (Power Device)	$P_{Conduct}$	P_{Switch}	P_{Total}	P_{arm}
IGBT 2-level Converter	2-level (IKW40N120T3)	45.837	47.04	92.877	92.877
MOSFET MMC	5-level (IPP200N25N3G)	18.2703	1.1627	**P_{cell}** 19.433	**P_{arm}** 77.732
	7-level (IPP110N20N3G)	11.8787	0.2089	12.088	72.526

Table 1: 2-level converter and MMC power loss (Watts)
P_{Total}=combined IGBT and freewheel diode loss; P_{arm}=total power loss for devices in one MMC arm; P_{cell}= power loss in one MMC cell.

These results show that the power loss in the MMC is less than that for conventional IGBT-based 2-level converter. The MMC is therefore selected for further study.

3 MMC Control

The main considerations for MMC control are (1) cell capacitor voltage balance, (2) power loss minimisation, (3) minimisation of circulating current, and (4) independent and minimal cell control. In this section, several control methods are analysed and simulation results are presented.

3.1 The capacitor balancing control

Similar to other multilevel topologies, each capacitor voltage must be controlled and equalised [11]. As stated in Section 2.3.2, the PD-PWM method determines the number of cells that should be turned-on in one phase of the MMC. For PhS-PWM, the switch on and off states are defined after each carrier is arranged. PD-PWM and PhS-PWM control strategies are analysed in detail.

3.1.1 The PD-SPWM based balancing strategy

For an MMC, when arm current is positive, if a cell in the arm is on (i.e S_{xi} is on in Figure 3), the corresponding capacitor will be charged and its voltage (V_{ci}) increases. When the arm current in negative, the capacitor will discharge and V_{ci} decreases. If a cell is off (i.e. S_{xi} is off in Figure 3), the corresponding capacitor will be bypassed regardless of arm current direction, and its voltage will be unchanged [12].

The PD-SPWM based balancing strategy is summarised as:

(1) Capacitor voltages are periodically measured, and the upper arm group and the lower arm group are sorted in ascending order of voltage amplitude.
(2) During positive arm current, a switching state is selected to charge the capacitor having the minimum voltage. During negative arm current, a switching state is chosen to discharge the capacitor having the maximum voltage.

This control method is widely used in MMC, especially in HVDC applications. However, it requires all capacitor voltages to be compared, meaning that the control method is not independent.

3.1.2 The PhS-SPWM based individual balancing control

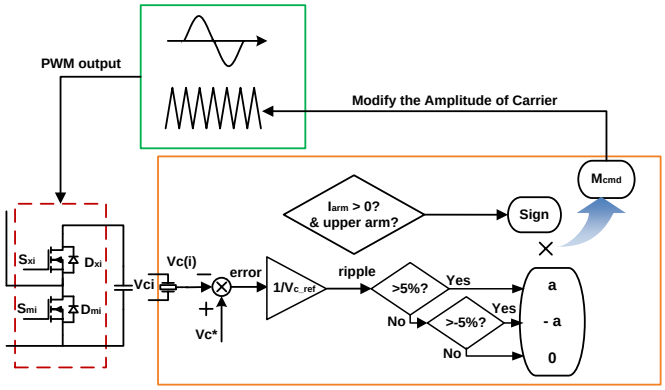

Figure 7: PhS-PWM MMC individual balancing control block

In Figure 7, capacitor voltage is measured and compared with a reference. If the error is within ±5%, no control signal is generated. If it is outside this 5% band, a compensation signal (±a) is generated. According to the direction of arm current, this signal is either added to or subtracted from the amplitude of the corresponding carrier to modify the modulation index. In this way, the duty cycle of each cell can be changed to achieve appropriate capacitor charge and discharge. The inputs to this controller are its own capacitor voltage and arm current, thus giving independent cell control.

The modulation index of PhS-SPWM control is expressed as:

$$M = \frac{A_m}{A_c} = \frac{A_m}{A_{c0} + M_{cmd}} \quad (35)$$

where M_{cmd} is the compensating signal.

Equation (35) highlights the reciprocal relationship between compensating signal M_{cmd} and modulation index M. Thus, a positive value of M_{cmd} will decrease modulation index.

If V_c is much less than V_{c_ref} and i_{a1}>0, the capacitor should be charged for longer, i.e. the duty cycle of S_{xi} in Figure 3 is increased. If i_{a1}<0, the capacitor should be discharged for a shorter time, i.e. the duty cycle of S_{xi} is decreased.

As shown in Figure 8, if an increase in upper arm S_{xi} duty cycle is required, $M\sin\omega t$ should be reduced. When $\sin\omega t>0$, M should be reduced. According to (35), a positive compensating signal M_{cmd} is therefore required. Other cases are determined using the same method.

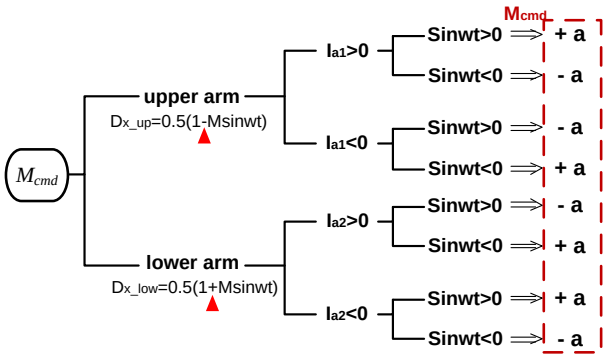

Figure 8: Polarity of compensating signal m
D_{x_up} and D_{x_low} are the duty cycles of upper and lower arm S_{xi} respectively; 'a' is the absolute value of compensating signal

Simulation results for a 5-level MMC are shown in Figures 9-11. The input DC side voltage is 600V and the switching frequency is 10kHz. The converter is rated at 10kW.

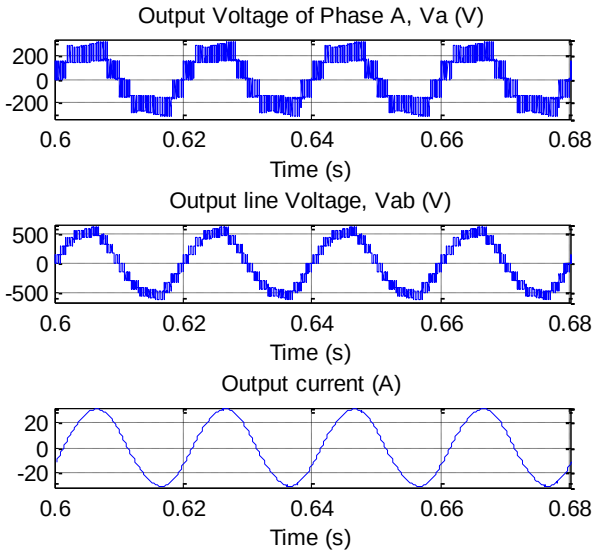

Figure 9: 5-level MMC output voltage and current waveforms

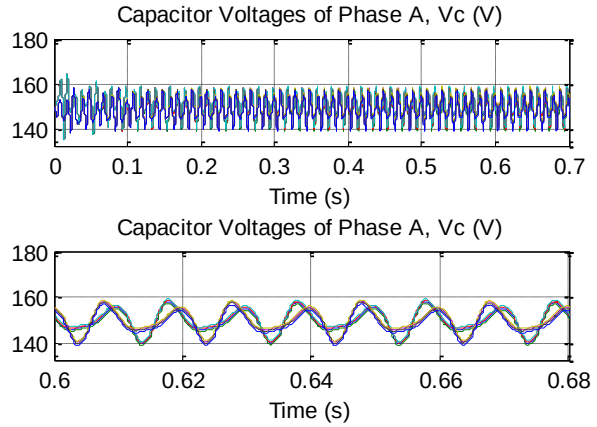

Figure 10: Phase 'a' capacitor voltages (8 cells)

Figure 10 shows the well-balanced capacitor voltages in a 5-level converter. In Figure 11, one capacitor with a 20V DC offset is balanced after 0.4s using PhS-PWM based individual control.

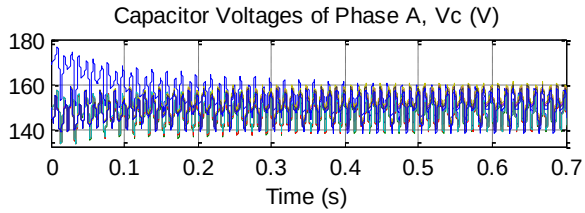

Figure 11: Capacitor voltages with a 20V offset in one cell

3.2 The elimination of input DC current distortion

Mathematical analysis [10], has shown the 2nd harmonic to be the most significant component in the circulating current. Circulating current i_{az} can therefore be expressed as:

$$i_{az} = I_{az}\sin(2\omega t + \theta) \tag{36}$$

In a 3-phase system with a balanced load, the DC-side ripple current ΔI_{dc} can be calculated as:

$$\Delta I_{dc} = i_{az} + i_{bz} + i_{cz} = I_{az}\sin(2\omega t + \theta) + I_{bz}\sin(2\omega t + \theta + 240^{o}) + I_{cz}\sin(2\omega t + \theta + 120^{o}) \tag{37}$$

If the load is well balanced ($I_{az} = I_{bz} = I_{cz}$), the DC-side current will not have a 2nd harmonic component. For an H-bridge inverter, however, the DC-side current will see a large 2nd harmonic component.

$$\Delta I_{dc} = i_{az} + i_{bz} = I_{az}\sin(2\omega t + \theta) + I_{bz}\sin(2(\omega t + 180^{o}) + \theta) \tag{38}$$

Assuming that $I_{az} = I_{bz}$, the DC-side ripple current will be

$$\Delta I_{dc} = 2I_{az}\sin(2\omega t + \theta) \tag{39}$$

From (39), the DC-side current is doubles that of the circulating current in each phase.

To eliminate the 2nd harmonic component, the proportional resonant (PR) control method is introduced, as shown in Figure 12. According to (27) and (28), the sum of i_{a1} and i_{a2} is twice the circulating current i_{az}. A PR controller introduces an infinite gain at a selected resonant frequency (100Hz in this case) to eliminate the current harmonic at that frequency [13].

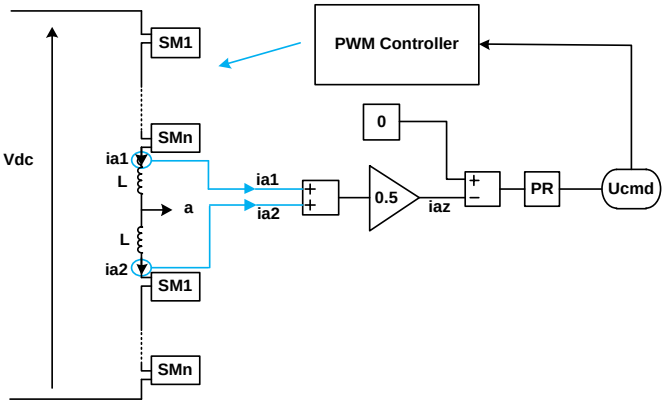

Figure 12: PR controller for MMC

Figure 13 and Figure 14 show simulation results of input current without and with a PR controller respectively. Comparing these two waveforms, it can be concluded that the PR controller has a significant effect on elimination of 2nd harmonic distortion.

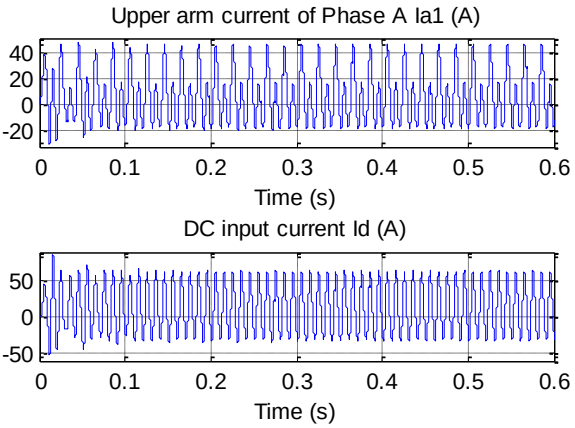

Figure 13: Current waveforms without a PR controller

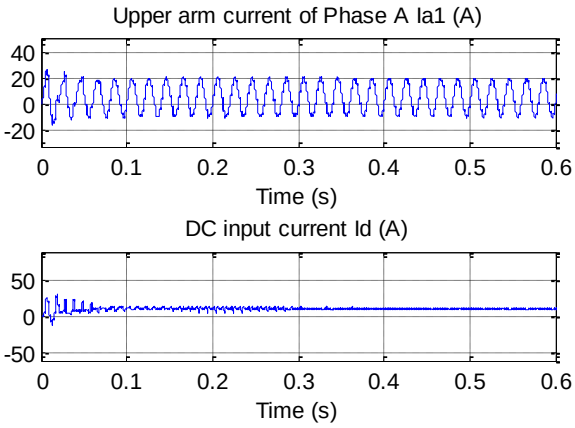

Figure 14: Current waveforms with a PR controller

4 Conclusion

A low-voltage MOSFET-based MMC for application in a LVAC distribution system is investigated. Power losses in a MOSFET-based MMC and in a conventional IGBT-based 2-level converter have been calculated and compared. Results show that the total loss in the MOSFET-based MMC is lower than that in the conventional IGBT-based converter. PD-PWM and PhS-PWM based capacitor voltage balancing strategies for MMC used in an LVDC system are presented and evaluated. A method to eliminate 2nd harmonic circulating current is also presented. The study shows that PhS-PWM based individual control with a PR controller can effectively provide voltage balancing for the MMC and eliminate DC-side current distortion. Future work will include development of a hardware demonstrator and practical verification of the individual control strategy.

Acknowledgements

The authors gratefully acknowledge the financial support of the EPRSC (www.epsrc.ac.uk, Grant No. EP/I031707/1).

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